Notice

The information in this guide is subject to change without notice.

COMPAQ COMPUTER CORPORATION SHALL NOT BE LIABLE FOR TECHNICAL OR EDITORIAL ERRORS OR OMISSIONS CONTAINED HEREIN; NOR FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES RESULTING FROM THE FURNISHING, PERFORMANCE, OR USE OF THIS MATERIAL.

Technical Reference Guide

Compaq Armada E500 and Armada V300 Series

First Edition March 2000
Part Number 11QY-0200A-WWEN

Compaq Computer Corporation

preface

REFERENCE DOCUMENTS

The following reference documentation and web addresses provide information for the Compaq Armada E500 and Armada V300 computers:

- Compaq Specification

  #333116, *ATI Rage Mobility-P Video Controller*

  #353918, *TI PCI1450 Cardbus Controller*

  #342609, *ESS 1978SF Maestro-2E Audio Controller*

  #387046, *SMSC MSIO, SMSC37N971, Tikki*

  #290725, *Flash ROM,512k x 8, 60ns, 5V*

  #353924, *ESS 1920 Audio Codec*

  #258896, *Li-Ion Battery Specification*
- *Compaq Armada E500 and Armada V300 Maintenance and Service Guide*
- *Microsoft Operating System Manual*
- *Synaptics Touchpad Interfacing Guide*
- Compaq Web site at http://www.compaq.com
- Modem commands at http://www.compaq.com/support/portables

CONTENTS

chapter 1

SYSTEM ARCHITECTURE

The Compaq Armada E500 and Armada V300 Series offer Intel Mobile Pentium II, III or Celeron Processors with 32-bit or 64-bit architecture, MMX technology, and level-2 cache memory. Both Armada E500 and Armada V300 Series provide desktop functionality and connectivity through optional expansion bases or convenience bases.

Depending on the Armada E500 computer model, the following processors are used:

- a 366- or 400-MHz Intel Mobile Pentium II Processor with 256-KB integrated L2 cache, or
- a 450-, 500-, or 600-MHz Intel Mobile Pentium III Processor with 256-KB integrated L2 cache.

Depending on the Armada V300 computer model, a 400- or 466-MHz Intel Celeron Processor with 128-KB integrated L2 cache is used.

The computers, shown in Figure 1-1, dock with the Compaq ArmadaStation EM (Armada E500 only), Armada MiniStation E/EX (Armada E500 only), Convenience Base or Port Replicator.

Figure 1-1. *Compaq Armada E500 and Armada V300 Personal Computers*

Standard Features

The computers have the following features:

- The following processors are available, varying by computer model:
  - The Armada E500 features an Intel Mobile Pentium III 450-, 500-, or 600-MHz Processor or Intel Mobile Pentium II 366- or 400-MHz Processor, with 256-KB integrated cache.
  - The Armada V300 features an Intel Celeron 400- or 466-MHz Processor, both with 128-KB integrated L2 cache.
- ATI Mobility P video controller, with 8-MB (Armada E500) and 4-MB (Armada V300) SGRAM (synchronous graphics)
- The following standard memory is available, varying by computer model:
  - The Armada E500 is equipped with 64-MB high-performance Syncheronous DRAM (SDRAM), expandable to 512 MB.
  - The Armada V300 is equipped with 64- or 32-MB high-performance SDRAM, expandable to 512 MB.
- Microsoft Windows 95, Window 98 or Windows NT Workstation 4.0 preinstalled
- The following displays are available, varying by computer model:
  - The Armada E500 features a 15-inch or 14.1-inch, XGA, TFT (1024 × 768) or 12.1-inch, SVGA, TFT (800 × 600) display, both with over 16.8 million colors.
  - The Armada V300 features a 14.1-inch XGA TFT (1024 × 768), 12.1-inch SVGA TFT (800 × 600), or 12.1-inch SVGA STN (800 × 600) display, all with over 16.8 million colors.
- The following keyboards are available, varying by computer model:
  - The Armada E500 provides a TouchPad or pointing stick keyboard.
  - The Armada V300 is equipped with a TouchPad keyboard.
- Mini PCI 56K V.90 modem, optional Mini PCI V.90 modem plus 10/100 NIC combination card.
- The following PC Card features are available, varying by computer model:
  - The Armada E500 features two Type II PC Card slots with support for both 32-bit CardBus and 16-bit PC Cards; Zoomed video is supported in the bottom slot.
  - The Armada V300 features one Type II PC Card slot with support for both 32-bit CardBus and 16-bit PC Cards.
- External AC adapter with power cord
- The following battery packs are available, varying by computer model:
  - The Armada E500 supports a 9- or 6-cell Lithium Ion (Li-ion) primary battery pack in the battery bay or DualBay, and a 6-cell Li-ion MultiBay battery pack in the MultiBay; supporting up to three battery packs in the computer at one time.
  - The Armada V300 supports a 9- or 6-cell Li-ion primary battery pack in the battery bay and a 6-cell Li-ion MultiBay battery pack in the MultiBay.

- The following hard drives are available, varying by computer model:
  - The Armada E500 supports a 12.0-, 6.0-, or 4.3-GB high-capacity SMART hard drives with DriveLock security and Prefailure Warranty.
  - The Armada V300 supports a 6.0- or 4.3-GB high-capacity SMART hard drives with DriveLock security and Prefailure Warranty.
- Flexible MultiBay that accommodates a 24X MAX CD-ROM drive, DVD-ROM drive, SuperDisk LS-120 drive, 6-cell Li-ion MultiBay battery pack, or secondary hard drive (when used with a Hard Drive MultiBay Adapter).
- Armada E500 provides a DualBay that accommodates a diskette drive or a second battery pack.
- Connectors for parallel, serial, audio in/out, external monitor, universal serial bus, external keyboard, and AC power.
- Stereo speakers providing Compaq PremierSound 16-bit stereo sound.
- Energy Star-compliant power saving features.
- Security features, including power-on, keyboard, setup, and DriveLock passwords.
- Desktop expandability available with the optional Compaq Armada Station EM and Compaq Convenience Base.

External Ports/Connectors

- Standard 176-pin Armada docking connector
- Fast IR port
- One or two CardBus slots with support for Zoomed Video
- Audio connectors for speaker or headphones out, and microphone in
- PS/2 port for mouse or external keyboard with support for Y–cable for two devices
- RJ-11 modem jack with internal connection to modem slot, depending on model
- RJ-45 Ethernet jack with internal connection to the combination modem/LAN slot, depending on model
- One standard 15-pin VGA connector with support for DDC-2B monitor detection
- One standard 9-pin serial port connector
- One standard 25-pin parallel port connector with support for ECP, EPP, bidirectional, and standard mode
- One low-power USB port with standard Type–A connector

Power Management

- Advanced Power Management (APM) version 1.2 compliant
- Advanced Configuration and Power Management (ACPI) version 1.0 compliant
- Support for Suspend (S1), Suspend-to-RAM (S3), and Suspend-to-Disk (S4)
- Power management settings can be customized by the user
- Hotkeys for setting performance level versus battery life
- Smart batteries that provide an accurate battery power gauge
- Dock device power management
- Active Thermal Feedback (ATF) support
- Lid switch suspend/resume
- Power/Suspend button with system override

System Architecture

The system architecture is shown in Figure 1-2.

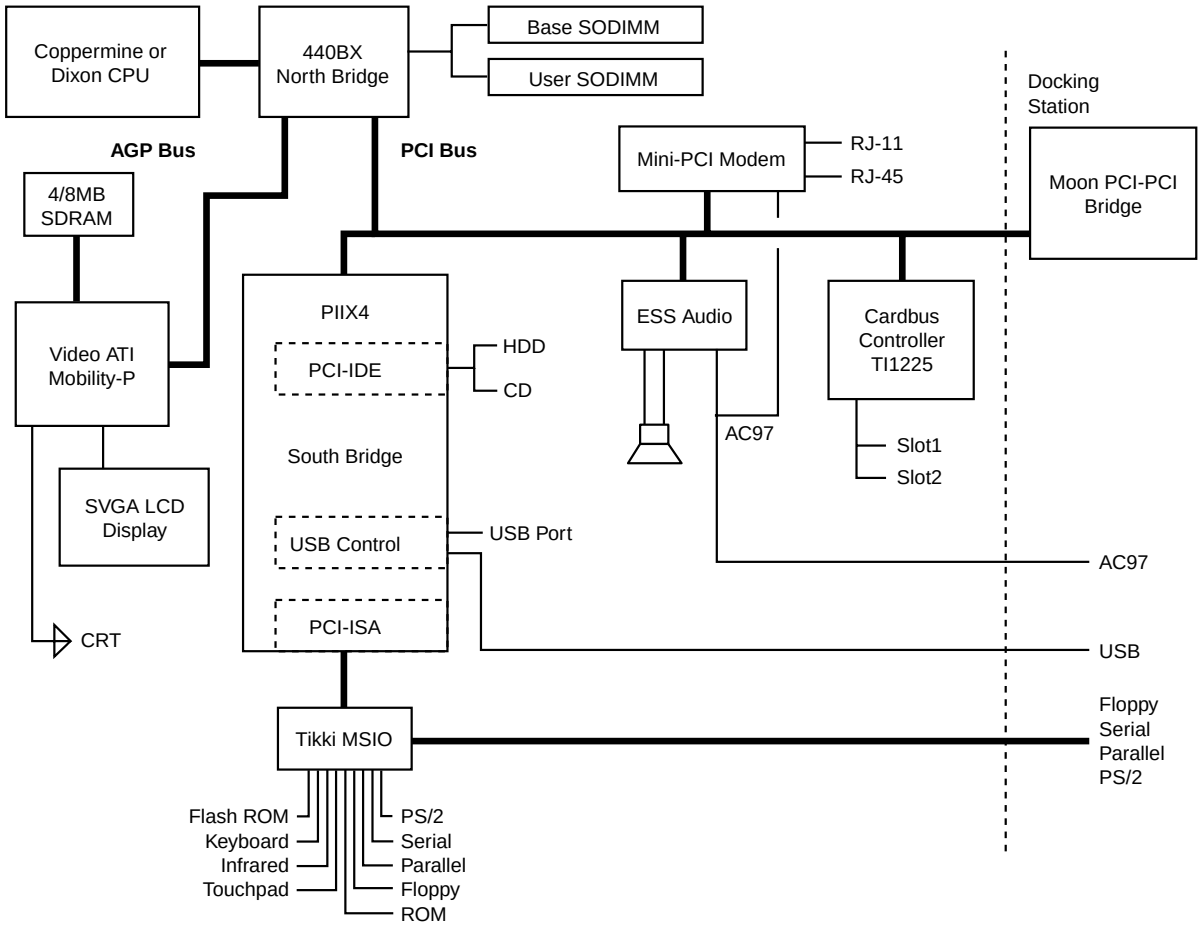

Figure 1-2. *Compaq Armada E500 and Armada V300 Block Diagram*

The system is made up of four main buses: the host bus, the AGP bus, the PCI bus, and the ISA bus. The Intel 440BX chipset controls all four buses. The 82440 interfaces the host bus to the AGP and PCI buses and is referred to as the Northbridge. The PIIX4E, used with the PII, or the PIIX4M, used with the PIII, interfaces from the PCI bus to the ISA bus and is referred to as the Southbridge.

The host bus is connected to:

- Celeron, Pentium II, or Pentium III processor
- Secondary cache (L2)
- Northbridge chipset (82440BX)

The AGP bus is connected to:

- Northbridge chipset (82440BX)
- Video controller (ATI RAGE Mobility-P)
- System SDRAM

The PCI bus is connected to:

- Northbridge chipset (82440BX)
- Southbridge chipset (PIIX4M)
- CardBus controller
- Audio subsystem

The ISA bus is connected to:

- Southbridge chipset (PIIX4M)
- Flash ROM
- Super I/O controller (MSIO)

CPU

Armada E500:

- 366- or 400-MHz Intel Mobile Pentium II Processor
- 450-, 500-, or 600-MHz Intel Mobile Pentium III Processor

Armada V300:

- 400- or 466-MHz Intel Celeron Processor with 128-KB integrated L2 cache

Chipset

Intel 82440BX Northbridge

- Support for all Intel Mobile Pentium II and Pentium III Processors
- Unbuffered and registered SDRAM support (×-1-1-1 access at 66 to 100 MHz)
- Enhanced SDRAM Open Page Architecture support for 16- and 64-Mbit DRAM devices with 2-, 4-, and 8-Kbyte page sizes
- PCI bus interface
    - PCI revision 2.1, 3.3-volt, 33-MHz interface compliant
    - PCI Parity Generation support
    - Data streaming support from PCI to DRAM
    - Delayed transaction support for PCI-DRAM reads

- AGP interface
  - Integrated DRAM controller supports single AGP-66/133 compliant device (3.3 volt)
  - AGP Specification revision 1.0 compliant
  - AGP data/transaction flow optimized arbitration mechanism
  - AGP side–band interface for efficient request pipelining
  - AGP specific data buffering
  - Supports concurrent CPU, AGP, and PCI transactions to main memory
  - AGP high-priority transaction support
- Advanced power management features
  - Supports Standby (S1), Suspend-to-DRAM (S3), and Suspend-to-Disk (S4)
  - Static stop clock support
  - Dynamic power-down of idle DRAM rows
  - SDRAM self-refresh power-down support in suspend mode
  - Stop clock grant and halt special cycle translation (host to PCI Bus)
  - Advanced Configuration and Power Interface (ACPI)–compliant power management
- 492-pin BGA package
- 3.3-volt core and mixed 3.3-volt and GTL I/O
- Interfaces directly to the PIIX4M

Intel PIIX4M Southbridge

- 3.3-volt with 5-volt tolerance
- PCI-to-ISA bridge
  - Supports full ISA or Extended I/O (EIO) bus in positive decode or subtractive decode
  - Supports PCI DMA with three PC/PCI channels and Distributed DMA protocols (simultaneously)
  - Supports serialized IRQ protocol
  - PCI revision 2.1 specification compliant
- Built-in real-time clock with wake-on-alarm capability (ACPI/OnNow compliant)
- SMBus interface

- Advanced Power Management support
  - 3.3-volt operation with 5-volt tolerant buffers
  - Power-On Suspend (S1), Suspend-to-DRAM (S3), Suspend-to-Disk (S4), and Soft-Off (S5) System States
  - All registers readable and restorable for proper resume from zero-volt suspend
  - Global and local device management
  - Supports thermal alarm
  - Support for external microcontroller
  - Full support for ACPI revision 1.0 specification and OS directed power management
- Integrated IDE controller with Ultra-DMA-33 support
  - Integrated 12 × 32-bit buffer for IDE PCI burst transfers
- Two hot-swappable USB channels with legacy keyboard/mouse support
- 324-pin mBGA package

DRAM

- 64-MB synchronous DRAM (SDRAM) memory onboard
- Two SO-DIMMs (Bank 1 and 2)
- All DRAM is 3.3-volt 66-MHz or faster self-refreshing SDRAM

PCI Bus Devices

NOTE: All internal PCI buses and PCI components operate at 3.3 volt.

- CardBus controllers

  TI225

  - Support for Zoomed Video slot
  - Support for serialized ISA IRQs
  - Supports two PC Card/CardBus slots (one PC Card slot for Aramada V300) with hot removal/insertion
  - Burst transfers to maximize data throughput on the PCI/CardBus bus
  - Supports distributed DMA and PC/PCI DMA
  - Supports ring indicate

- Video Controller

  ATI RAGE Mobility-P

  - 32-bit wide memory-mapped registers
  - Advanced Graphics Platform (AGP) 2X bus with sideband support; 133-MHz throughput
  - Floating-Point Setup Engine for high-performance 3D and CAD
  - Motion compensation for full-screen MPEG-2 video without external acceleration hardware
  - 4 or 8-MB, 3.3-volt 125-MHz video SDRAM
  - Support for Zoomed Video
  - Built-in support for LVDS data bus to LCD display
  - Built-in NTSC and PAL video output (composite)
  - Simultaneous display of CRT+LCD+TV including separate images
  - DDC 2B support for external monitors
  - Advanced power management features (automatic power-down, standby, and panel-off)

- Audio

  ESS Maestro 2E/ES1921 CODEC

  - Hot docking 6-pin interface to expansion audio mixer (ES978)
  - Monophonic full duplex using two DMA channels
  - Self-timed joystick port
  - I^2S interface to internal stereo D/A for external ZV port
  - Complete general interrupt mapping, including sharing of all interrupts
  - Stereo 16-bit, Wavetable and FM synthesizers, MPU-401 MIDI support

ISA Bus Devices

NOTE: All internal ISA buses and ISA components operate at 3.3-volt.

- BIOS ROM

  Intel 28F004BV

  - 4-MB boot block flash ROM

- SMC Super I/O Controller

  SMC FDC37N97X

  - Simultaneous support for three PS/2 ports (1 internal + 2 external)
  - Advanced infrared communications controller
  - ACPI Embedded Controller Interface
  - High-performance, embedded 8051 keyboard and system controller
  - Low Suspend current in sleep mode
  - System power plane control and power sequencing
  - Battery management interface for charging and smart battery fuel gauge
  - Active thermal interface for CPU thermal management
  - 1.44-MB Super I/O FDC controller
  - IEEE 1284 parallel port
  - Serial infrared support: IrDA version 1.1 (4 Mbps)
  - Full Plug-and-Play support
  - High speed NS16550A-compatible UART with 16-byte send/receive FIFOs
  - Real-time clock
- Modem/LAN

  Mini-PCI Modem or Combination Modem/NIC Card

  - Internal Mini-PCI Type-1B slot
  - Flexible method of supporting an internal modem or modem/LAN combo card with the least amount of difficulty surrounding European modem approvals
  - Slot supports only Compaq-approved cards

Power Subsystem

- System DC/DC
  - Based on the MAX1630
  - Provides a stable 3.3 to 5.0 volts from a DC source of 9 V to 19 V
- AC Cube
  - Provides 18.5 volts DC +/- 3.75% at 100 to 240 volts AC
  - 50 watts output
- 6 or 9-cell Li-ion battery in dedicated bay; only Armada E500 and Armada V300-specific batteries can be inserted into the primary bay due to mechanical keying

Mechanical

- Size: 9.9-in (252 mm) × 12.36-in (314 mm) × 1.65-in (42 mm)
- Weight: 5,5 to 7.5 pounds (2.6 to 3.2 kg)
- Construction: 2.3 mm wall thickness using polycarbonate
- Features:
  - One MultiBay for SuperDisk LS-120 drive, DVD-ROM drive or second hard drive; one DualBay that can be used for a diskette drive/battery on the Armada E500; one fixed diskette drive on the Armada V300
  - Removable main hard drive
  - Easy-to-access memory upgrades
  - Ergonomic design

Docking Support

ArmadaStation EM Support (Armada E500 only)

- One serial port
- One parallel port
- Two PS/2 ports to connect an external keyboard and a pointing device
- One XGA CRT port (replicates computer port)
- Three PCI slots for Compaq-approved PCI add-in cards
- Dual MultiBays
- One half-height bay
- An additional dual-channel, PCI-based IDE controller, to connect HDD, CD-ROM, DVD-ROM,or other peripherals
- Audio line-in, microphone-in, speaker/headphones-out
- Additional audio speaker
- Two USB ports

Convenience Base

- One serial port
- One parallel port, with support for an Armada 4100/7800-compatible diskette drive option (Note: The Armada E500 and Armada V300 do not support this, but the Convenience Base does.)
- Two PS/2 ports to connect one for an external keyboard and a pointing device
- One XGA CRT port (replicates computer port)
- One PCI slot capable of supporting Compaq-approved LAN adapters
- Audio line-in, microphone-in, speaker/headphones-out
- Two USB ports

Port Replicator

- One serial port
- Two PS/2 ports to connect an external keyboard and a pointing device
- One XGA CRT port (replicates computer port)
- Audio line-out
- One USB port
- DC power-in (pass through)

Security Features

These security management features customize system security:

- Power-On and Setup Passwords—prevent unauthorized access to information and computer configuration.
- DriveLock—prevents unauthorized access to hard drives.
- Device disabling—prevents unauthorized data transfer through modems, serial ports, parallel ports, and infrared ports on the computer and an optional docking station.
- QuickLock/QuickBlank—locks the keyboard and clears the screen.
- Ownership Tag—displays ownership information during system restart.

chapter 2

PROCESSOR, CACHE, AND SYSTEM SUPPORT

Host Bus (Northbridge)

The Armada E500 and Armada V300 computers use the Intel Pentium II, Pentium III, and Celeron Processors, respectively. The Pentium Processors feature:

- 450-, 500-, or 600-MHz CPU with 100-MHz SDRAM bus for PIII, 66MHz for PII
- Integrated L2 cache running at processor speed
- MMX-2 instruction set
- SpeedStep desktop operation (PIII)

Pentium II or III CPU/Cache

The computers use the Intel Pentium II or III Processor technology housed in a BGA package. The PII and PIII differ in substantial ways (66-MHz bus instead of a 100-MHz bus, integrated GTL resistors) so that a common PII and PIII printed circuit board is impossible. A general feature list is as follows:

- Full SMI (System Management Interrupt)
- Fully static (support Stop grant and Stop clock states)
- 66- (PII) or 100-MHz (PIII) bus interface to the system
- 32-bit address bus
- 64-bit data bus
- 256-KB on-chip cache (Armada E500 PII and PIII); 128-KB on-chip cache (Armada V300)
- Capability of executing two instructions per clock through two pipelined integer units
- Multimedia extension (MMX) register set

The PII Processor has integrated 256 K L2 cache on the die designed using 0.18 micron process technology. It is offered at 400- and 466-MHz with 66-MHz system bus speed. It's core design consists of an integrated L2 cache controller and a 64-bit high performance system bus. The on-die L2 cache complements the system bus by providing critical data faster, improving performance, and reducing total system power consumption. The PII Processor's 64-bit wide low power GTL+ system bus is compatible with the 440BX PCIset and provides a glueless, point to point interface for an I/O bridge/memory controller.

The Intel Pentium III Processor also implements 0.18 micron process technology with Katmai New Instructions. It has a 100 MHz bus and uses the PIIX4M and 440BX chipset with 100 MHz SDRAM.

The new Intel SpeedStep technology allows the PIII Processor to run at either notebook or desktop frequencies. At the higher frequency, a higher voltage must also be run. For the Armada E500, the notebook frequency is 500 MHz at 8 watts, and the desktop frequency is 650 MHz at 14 watts. The high power mode may be operated under battery or AC power, but the battery life will be lower and the acoustic noise higher than operation in the normal notebook mode.

The Intel PII and PIII Processors are fully compatible with the entire installed base of applications for DOS, Windows, OS/2, and UNIX. Superscalar architecture, branch prediction, and separate code and data caches all provide increased performance over previous X86 Processors. Reduced voltage operation and enhanced power management features are provided.

82440BX

The Intel 440BX PCI-based chipset is optimized for portable systems with stringent form-factor and power-consumption requirements. It consists of two components–the 82440BX and the PIIX4M. The 82440BX is referred to as the Northbridge (control between the PCI bus and the CPU and AGP buses). The PIIX4M is referred to as the Southbridge (control between the PCI bus and the ISA bus). The remainder of this section involves the 82440BX.

The 82440BX integrates the CPU, AGP, PCI, and DRAM bus interfaces. This includes the DRAM controller, AGP bus arbiter, PCI bus arbiter, power management, and the host (CPU) interface.

The 82440BX's data buffer steers and buffers data between the four interfaces: 64-bit CPU, 64-bit DRAM, 32-bit AGP, and 32-bit PCI. The data flow can be CPU-to-PCI, CPU-to-AGP, CPU-to-DRAM, AGP-to-DRAM, or PCI-to-DRAM.

Power Planes

The 82440BX supports suspend modes: Power-On-Suspend (POS), Suspend-To-RAM (STR) and Suspend-To-Disk (STD). The 82440BX maintains leakage control so that back powering of other system functions cannot occur in Suspend. Table 2-1 lists the 82440BX power planes.

Table 2-1
82440BX Power Planes

Plane	VCC OPTIONS	Selection	Description
VCC	3.3 V	BXVCC3	Main power pin at 3.3 V
VCCAGP	3.3 V	BXVCC3	AGP bus power
GTLREFA,B	0.55 VTT	VBXGTLREF	GTL buffer voltage reference input
VTTA,B	CPU selected	VBXGTL	GTL threshold (clamp) voltage
REFVCC5	3.3 V	BXVCC3	PCI 5 V tolerant level (not used)

Reset Interface

The 82440BX reset function is an integral part of the Suspend/Resume functions. The 82440BX supports the normal reset function in a desktop platform, as well as various power-up reset and resume reset functions in the mobile platform.

The PIIX4M integrates the system reset logic for the system. The PIIX4M generates PCIRST# and RSTDRV during power up (PWROK), when a hard reset is initiated through the RC register, and during certain power management resume operations.

The 440BX chipset has two separate reset inputs: RCIN# and PWROK; and four reset outputs: PCIRST#, CPURST#, SUS_STAT#, and INIT#.

PWROK: An RC delay from the enabling of SYSVCC3. During the period when RCRST# is de-asserted and PWROK is not yet asserted, RSTDRV and CPURST# are asserted. When PWROK becomes asserted, RSTDRV and CPURST de-assert, causing a system reset.

Table 2-2
440BX Reset Outputs

Signal	Assert w/ PCIRST#	System Devices or Buses Affected	Source	Description
PCIRST#	-	PCI bus, 82440BX, NB, PIIX4M	PIIX4M	Used in power-up sequence, resume from STR or STD.
CPURST#	Always	CPU	82440BX	CPU reset signal.
RSTDRV	Always	ISA bus / X-Bus devices	PIIX4M	ISA bus reset. Directly derived from PCIRST#. Resides in PIIX4M main voltage well.
SUSSTAT#	N/A		PIIX4M Only	SUSSTAT# signals a Suspend mode entry/exit. This signal originates from the PIIX4M Suspend voltage well.
INIT#	No	CPU	PIIX4M	CPU soft reset generated by PIIX4M.

CPURST# is generated by the 82440BX in the following instances:

- CPURST# is always asserted if PCIRST# is asserted.
- CPURST# is asserted during resume sequence from POS (CRst_En= 1).

The 82440BX de-asserts CPURST# 1 ms after detecting the rising edge of PCIRST#. The CPURST# is synchronous to the host bus clock.

The PCIRST# must be asserted when the system resumes from low power mode, in which power is removed, including resume from Suspend-to-RAM or Suspend-to-Disk and power-up sequence. In these cases, CPURST# is activated with the assumption that CPU power is removed to enforce correct resume sequence.

When resuming from POS, the PCIRST# and CPURST# typically are not used to speed up the resume sequence. In this case, the option to reset the CPU is available by using the CRst_En configuration bit option.

When a soft reset is initiated, the PIIX4M drives SUSTAT# to the 82440BX. This forces the 82440BX to switch to a Suspend refresh state. The 82440BX cannot accept BIOS attempts to execute cycles to DRAM because it believes it is in a Suspend state. After coming out of reset, software must set the Normal refresh enable bit (bit 4, Power Management Control register at Offset 7Ah) in the 82440BX before accessing memory.

Power-On Configuration

The 440BX chipset uses power-on registers to define system configuration variables that must be set by hardware options. All signals used to select power-on options are connected to either internal pull-down or pull-up resistors of minimum 50 K/maximum 150 K ohms. These resistors select a default mode on the signal during reset.

To enable different modes, external pull-up or pull-down resistors (the opposite of the internal resistors) of approximately 10 K ohm can be connected to particular signals. These resistors are connected to the +3.3-volt power supply. During normal operation of the 82440BX–including while it is in Suspend mode–the paths from GND or + 3.3 volts to the internal strapping resistors are disabled to effectively disable the resistors. In these cases, the MAB# lines are driven by the 82440BX to a valid voltage level.

Table 2-3 lists the Power-On options that are loaded into the 82440BX during cold reset. The 82440BX is required to float all the signals connected to straps during cold reset and keep them floated for a minimum of four host clocks after the end of cold reset sequence.

Table 2-3
82440BX Power-On Options During Cold Reset

Line	Setting	Description	Notes
MAB13#	-	Reserved	
MAB12#	0	Host frequency select	0 ***= 60/66 MHz, 1 **= 100 MHz
MAB11#	1	In-order queue depth enable	0 = non-pipelined, 1 ** = pipelined (8-deep)
MAB10	0	Quick start select	0 ** = normal mode, 1 = Quick start mode
MAB9#	0	AGP disable	0 ** = AGP enabled, 1 = AGP disabled
MAB8#	-	Reserved	
MAB7#	0	Memory module configuration	0 ** = normal (BX), 1 = 430TX-compatible
MAB6#	1	Host bus buffer mode select	0 ** = desktop GTL+, 1 = mobile GTL+

** default selection *** default on P-II versions ** default on P-III versions

When resuming from Suspend, even while PCIRST# is active, the MAB# lines remain driven by the 82440BX and the strapping latches maintain the value stored during the cold reset.

Clock Interface

The 82440BX requires two clock inputs which are CPUCLK (66 or 100 MHz) and PCICLK_440BX (33 MHz). The CPUCLK signal is buffered and driven DCLKOUT.

During certain conditions the CPUCLK signals may be stopped and restarted. The CPUCLK can be stopped in the sleep and deep-sleep modes and restarted when a primary activity is detected. The CPUCLK signal is driven in the On and POS states.

CPU Interface

The 82440BX Northbridge supports the Intel Mobile Pentium II/III Processor technology.

CPU address pipelining is supported. The ×-1-1-1 CPU writes can be supported up to 100 MHz. Write buffers exist for CPU-to-DRAM, CPU-to-AGP, and CPU-to-PCI cycles. Read re-ordering is supported for these buffers.

DRAM Controller

The DRAM controller supported by the 82440BX allows up to four 64-bit SDRAM banks for 512 MB. The DRAM controller supports synchronous DRAM (SDRAM).

For specifics on the computer's main memory, refer to the "System Memory" chapter in this document.

Secondary Cache (L2)

The Pentium II/III Processors support a 128/256-KB on-chip cache. The Processor module handles all control for the L2 cache. No external cache control logic or tag RAM memory is used.

PCI Bus

The PCI bus is a 32-bit, multiplexed address/data bus used for high-speed components. The PCI bus operates at half or one third of the CPU external clock rate. The PCI bus is clocked at 33 MHz. Bursting is supported from PCI bus masters into main memory.

PCI Slot Assignment

The PCI bus supports three cycle types: Memory, I/O, and Configuration. Configuration cycles are used to access the configuration registers in each PCI device. The only "address" associated with configuration cycles is an index into the configuration space composed of 256 32-bit registers. Selection of each PCI device is achieved by assigning each device a unique PCI slot number. This is accomplished in hardware by connecting the IDSEL pin of each device to a unique AD signal (AD0 - AD31); the same function is accomplished in the chipset by programming a decode that corresponds to the AD line.

PCI Bus Arbiter Scheme

The 440BX chipset supports up to five PCI master devices. One is dedicated to the PCI-to-ISA bridge in the PIIX4M. Because the PIIX4M acts for ISA and DMA masters, which do not support a preempt mechanism, the PIIX4M is not preemptable.

PCI Bus Power Management

The PCI Bus Power Management Interface Specification (PCIPM) establishes the infrastructure required to let the operating system control the power of PCI functions. This is done by defining a standard PCI interface and operations to manage the power of PCI functions on the bus. The PCI bus and the PCI functions can be assigned one of four software visible power management states, which result in varying levels of power savings.

The four power management states of PCI functions are: D0 (Fully On state), D1 and D2 (intermediate states), and D3 (Off state). Similarly, bus power states of the PCI bus are B0–B3. The bus power states B0–B3 are derived from the device power state of the upstream bridge device.

For the operating system to manage the device power states on the PCI bus, the PCI function should support four power management operations. The four operations are:

- Capabilities reporting
- Power status reporting
- Setting the power state
- System wake-up

The operating system identifies the capabilities of the PCI function by traversing the new capabilities list. The presence of new capabilities is indicated by a 1b in bit 4 of the PCI status register (PCI offset 06h). When software determines that the device has a capabilities list by seeing that bit 4 of the PCI status register is set, it will read the capability pointer register at PCI offset 14h. This value in the register points the location in PCI configuration space of the capabilities linked list.

The first byte of each capability register block is required to be a unique ID of that capability. The PCI power management has been assigned an ID of 01h. The next byte is a pointer to the next pointer item in the list of capabilities. If there are no more items in the list, the next item pointer should be set to 0. The registers following the next item pointer are specific to the function's capability.

The power management capabilities (PMC) register is a static read-only register that provides information on the capabilities of the function, related to power management. The PMCSR register enables control of power management states and enables/monitors power management events. The data register is an optional register that provides a mechanism for state-dependent power measurements such as power consumed or heat dissipation.

PIIX4M PCI Functions

While the primary function of the PIIX4M is to provide a bridge between the PCI and ISA buses, it also contains PCI devices and control logic. This section defines these PCI functions.

Distributed DMA and Serialized IRQ (DDMA) Support

Direct Access Memory (DMA) is an open standard that supports legacy devices on the PCI bus. The standard defines a method for supporting legacy DMA over the PCI bus with no additional signals. It also specifies a one-signal serialized IRQ scheme that allows ISA IRQ and PCI INTA-D to be sent over the signal pin interface.

The DMA standard specifies one “Master DMA” in the system. Each slave DMA device is assigned a base address at which to respond. The master DMA keeps a record of each slave DMA's base address. When accesses are performed to the standard DMA I/O space, the master DMA does a PCI retry, then gains control of the PCI bus and sends the cycle out itself to the assigned slave I/O addresses. The DMA slaves perform the actual DMA transfers themselves as standard PCI master cycles.

The serialized IRQ scheme uses a single pin interface (SERIRQ) that connects to each device supporting the scheme. Devices that support the SERIRQ scheme can generate IRQ15-IRQ0 and INTA-INTD.

PCI-IDE Controller

The PIIX4M includes a high-speed dual channel IDE interface that supports IDE devices, providing an interface for IDE hard disks, as well as other ATAPI-compliant IDE devices such as CD-ROMs. The IDE controller resides on the PCI bus and does not consume any ISA DMA resources.

Each IDE channel uses sixteen 32-bit buffers for optimal transfers. The IDE interface supports PIO IDE transfers up to 14 Mbytes/s and Bus Master IDE transfers up to 33 Mbytes/s (Ultra-DMA-33 compatible). Each IDE device can have independent timings.

The IDE pins of the PIIX4M are configured to the industry-standard Primary Master and Primary Slave (two devices). The computer models use the dual channel configuration with “legacy” resource allocation:

Table 2-4
PIIX4M Configuration

Resource	Primary IDE	Secondary IDE
Base I/O Address	1F0h	170h
IRQ	14	15

AGP Bus

The 82440BX supports a dedicated 66 MHz Accelerated Graphics Port (AGP) video bus. Like the PCI bus, the AGP bus is a 32-bit, multiplexed address/data bus, but it operates at 66 MHz–full or 2/3-CPU bus speeds, with bursting support into main memory. The AGP bus can only have two devices on it: the PCI-to-AGP bridge and the video controller.

Devices on the AGP bus can run in two modes:

- 1X speed – 66 MHz; one data window per clock pulse
- 2X speed – 66 MHz; data windows on both rising and falling clock edge; 133 MHz throughput

The computer supports both modes of operation and is compatible with the AGP Specification, revision 1.0.

Operation in 2X mode can reach peak transfer bandwidths in excess of 500 MB/s. (In comparison, PCI graphics controllers are limited to a peak bandwidth of 132 MB/s, which they must share with other PCI devices.) In addition, the video system supports AGP's pipelined sideband protocol, which improves the sustained bandwidth of data transfers, further enhancing video performance.

From a system-architecture point of view, the AGP bus looks exactly like a secondary PCI bus, and the AGP interface in the 82440BX appears to include a standard PCI-to-PCI bridge.

The main "behind-the-scene" differences are:

- The graphics controller is in sole possession of this bus, so bus arbitration is minimized.
- The AGP bus has a direct aperture into system DRAM, allowing quick access to large blocks of memory for 3D texture maps.

ISA Bus (Southbridge)

PIIX4M (82371EB)

The PIIX4M serves as the Southbridge, providing the following functions:

- Bridge between the PCI and ISA buses
- Logic to support master and slave cycles on both PCI and ISA buses
- Master power management controller for the 440BX chipset
- Mechanism to generate up to 53 general-purpose I/Os

Power Planes

The PIIX4M has a flexible power plane structure to support a wide variety of system configurations. Four independent power planes are used, plus a reference signal for communication to the ISA and PCI buses.

Table 2-5
PIIX4 Power Planes

	VCC options	Selection	Description
VCC	3.3 V	+ 3.3 V	Core voltage supply
VCCRTC	3.3 V	+ RTCVCC	RTC/CMOS logic power
VCCSUS	3.3 V	+3 VCC	Suspend Well logic supply
VCCUSB	3.3 V	+ 3.3 V	USB logic supply
VREF	5 V or 3.3 V	+ 5 V	External logic voltage reference

Clock Interface

Four clock signals are inputs to the PIIX4M:

- PCICLK_PIIX is used to create all PCI control signals. The PIIX4 also supplies the SYSCLK output for ISA devices derived from PCICLK_PIIX.
- USBCLK is used to derive all of the signals for the USB host adapter.
- 32 KHz is used to control the on-board RTC.
- 14 MHZ_PIIX4 is used to control the 8254-compatible timer in the PIIX4M.

Reset Interface

PCIRST# is used as the master reset signal for the PIIX4.

System Management Mode (SMM)

The PIIX4M provides a flexible System Management Mode (SMM) interface for both software and hardware. It can generate an SMI from many sources including:

- Power management events
- Timer time-outs
- Software triggered events

The SMM base address is defined as 000D0000H-000EFFFFH. The physical memory space used for SMM memory is at 000A0000H-000BFFFFH in DRAM.

SMRAM accesses are always marked as write-through to the L1 cache. SMRAM cannot be accessible by PCI or AGP masters.

Power Management Controller

The PIIX4M has the following power management functions designed to maximize system battery life:

- Enhanced clock control
- Local and global monitoring support and PMI generation for 14 individual on-board and system devices
- Advanced primary and secondary activity monitors
- Low-power states to provide battery conservation: power-on suspend, suspend-to-DRAM, and suspend-to-disk. These states and how they are applied to are discussed elsewhere in this document
- Hardware-based thermal management permitting software-independent entrance to low-power states
- Full support for the Advanced Configuration and Power Interface (ACPI) Specification
- Power management input from the Super I/O

PCI-to-ISA Cycle Translation

The PIIX4M has three physical address spaces: Memory, Input/Output, and configuration address spaces. A positive decoding scheme is implemented in PIIX4.

ISA Bus Interface

Although the computer is a PCI-based system, areas of ISA bus support are still required in the notebook and peripherals. To provide ISA bus support in the PCI system, a PCI-to-ISA bridge must be used to translate between the ISA and PCI buses. The PIIX4M provides this function.

The PIIX4 provides byte-swap logic, I/O recovery support, wait-state generation, and SYSCLK generation.

The PIIX4 can be configured as both a PCI-to-ISA bridge and as a positive decode bridge for PCI functions, such as the IDE controller and USB bus.

General Purpose Input/Output (GPIO) Usage

The PIIX4M provides up to 22 general purpose input (GPI) signals. These GPIs can be used to directly monitor system logic and external inputs. The read-only registers that store the state of these inputs are located in the PIIX4. See the 82371AB (PIIX4) design guide and 82371EB (PIIX4M) addendum for further information.

The PIIX4 also provides up to 31 general purpose output (GPO) signals. These GPOs can be used to directly monitor and control system logic. The read/write registers that store and change the state of these outputs are located in the PIIX4. See the 82371AB (PIIX4) design guide and 82371EB (PIIX4M) addendum for further information.

Some of these GPI and GPO pins are multiplexed with other PIIX4 functions. Depending on the PIIX4 features used, some of the GPIOs may not be available to the system.

The SMSC 37N971 Super I/O Controller provides eight general purpose input pins, ten general purpose outputs, and 22 general purpose I/O pins. Improvements on these pins are made for system management flexibility. The GPIO pins are controlled by the 8051, so that host access to them is through the mailbox registers. The host processor also has access to 16 GPIO pins that are in the PXII4. All of the GPIO pins that are located on the MSIO are as shown in Table 2-6.

Table 2-6
General Purpose Input Outputs (GPIOs)

Signal	Pin	Description	Location	Comment
STANDBY_SW#_3	148	Standby switch button	IN0(EE4)	Input
DCPRES_5	149	DC present indication for battery charge	IN1(EE2)	Input
LID_SW#_3	150	LID switch button	IN2(EE3)	Input
PWR_GOOD#_3	151	Power Good signal from DC/DC	IN3(GPWAKE)	Input from DC/DC, used for wakeup event initiated by PXII4 from STR. (RTC and RI).
ARB_IDLED_3	152	PLD output for notify idle	IN4(SE00)	Input
ERDY_5	153	Expansion Base Ready	IN5(SE01)	Input
EBOXS#_5	154	Expansion base present (short pin)	IN6(SE05)	Input
ACPRES_5	155	AC Power Present	IN7(EE1)	Input
RUNSCI_3	70	Runtime SCI	OUT0	Output, (initialized as “1” in VCC1 init routine.)
VGER_CLKEN#_3	71	Expansion clock enable for Vger type docking station.	OUT1	Output, (initialized as “1” in VCC1 init routine)
RSMRST#_3	72	Resume reset to PXII4	OUT2	Output
ADPTR_EN_5	74	Enable the AC-adapter	OUT3	Output (initialized as “1” in VCC1 init routine)
PCSPKC#_3	75	PC Speaker	OUT4	Output

Continued

Table 2-6 *Continued*

Signal	Pin	Description	Location	Comment
DS1#_5	2	Driver Selection for 2nd FDD	OUT5	Alt, Need configured this pin as DS1# in Vcc1 init.
MTR1#_5	3	Motor selection for 2nd FDD	OUT6	Alt, Need configured this pin as MTR1#
I2C_DCKEN_3	203	Enable Expansion I2C interface	OUT7	Output (initialized as "0" in VCC1 init routine. Level High to enable the Docking I2C interface)
KBCPURST#_3	23	Output to PIIX4 for Init generation	OUT8 (A) *	Output, Need to configured as KBD reset function.
JOUST_CKEN	201	Expansion clock enable for Joust type docking station	OUT9 (A)	Output, (initialized as "1" in VCC1 init routine, level low to enable the Arcade PCICLK)
FAN_PWM	200	Fan control for thermal	OUTA	Output, (initialized as PWM in VCC1 or VCC2 init)
INV_PWM_5	199	PWM for panel brightness	OUTB	Output, (initialized as PWM in VCC1 or VCC2 init)
FLASHCE#	184	Chip select for flash ROM	GPIO0 (HL3,SE)	Output, Do not change the default setting
MBAT	185	MBAT event	GPIO1 (HL4,SE)	Input
EBOXL#_5	186	Expansion base present (long pin)	GPIO2 (HL5)	Input
MB_SMI_3	187	SMI input from PLD for Multibay ID change.	GPIO3 (TRIG)	Input
SUSTAT2#_3	188	Early suspend and late resume indication	GPIO4	Input
PWR_SWIN#_3	189	Power switch button input.	GPIO5	Input
IR_SD	190	FIR Mode Control	GPIO6	Output, Need to configure it as FIR mode function
FLASHPGM_3	191	Flash VPP On	GPIO7	Output
AUXBAT_FCHG_3	141	Fast charge the Aux battery	GPIO8	Output
LOW_BAT#_3	142	Low battery signal indication	GPIO9	Output, Need to initialize as high in VCC1 init.
PCI_EXP#_3	145	Enable docking Q switch	GPIO10	Output, Need to initialize as high in VCC1 init.
SDA_IO2	146	Second I2C Data bus in the MSIO	GPIO11	Input/Output, Need to enable it in VCC1 init
SCL_IO2	147	Second I2C Clock	GPIO12	Input/Output, Need to enable it in VCC1 init
8051_A18	144	Address bit A18 for ROM	GPIO13	Output, Do not change the default setting, configured as A18
PWR_SW#_3	140	Power button output to PXII4	GPIO14	Output, Need initialize as high in VCC1 init
SRDY_3	139	System Ready to expansion	GPIO15	Output
CAPS_LED#_3	204	Cap lock LED/(ID0)	GPIO16	Output/input, ID0 is strapped high

Continued

Table 2-6 *Continued*

Signal	Pin	Description	Location	Comment
A20GATE_3	206	A20 Gate to PIIX4 A20 input	GPIO17	Output, Need to configure it as A20 function in VCC1 init.
IDLE_ARB_3	22	Output to PLD for idle PCI bus	GPIO18 *	Output, Need to initialize as low in VCC1 init.
ARCADE_EN#_3	208	Enable the Mux for Arcade mode	GPIO19	Output, Need to initialize as high in VCC1 init
NUM_LED#_3	45	NUMLock led / (ID1)	GPIO20	Output/ Input, ID1 is strapped high
SCROLL_LED#_3	46	SCROLL lock Led / (ID2)	GPIO21	Output/input, ID2 is strapped high
RESET_OUT#	102	System Reset	RESET_OUT	
PWR_LED#	110	Power LED	nPOWER_LED	
BAT_LED#	197	Battery Charge LED	nBAT1_LED	
FDD_BAT_LED	198	MultiBay LED	FDD_BAT2_LED	

System Interrupt Map

The interrupt usage of a PCI/PnP system can vary considerably and is based on the commands given by the OS during hardware detection and configuration. The following default interrupts are set on the system. Some interrupts, while immovable, can be disabled, freeing up the resource. Table 2-7 lists the system interrupts.

Table 2-7
System Interrupts

IRQ	Use
0	System timer
1	Keyboard
2	Cascade for interrupts 8-15
3	Serial IRQ for Com 2 and 4
4	Serial IRQ for COM 1 and 3
5	Reserved for ESS Audio
6	Diskette controller
7	Parallel port
8	Real-Time Clock
9	ACPI SCI interrupt
10	CardBus
11	PCI IRQ
12	PS/2 for pointing device
13	Numeric Processor
14	Primary IDE controller
15	Fast Infrared

Real-Time Clock

The real-time clock (RTC) functions are provided in a special area of the PIIX4M containing low-power CMOS circuitry that keeps the current time and date and a low-power CMOS storage area for system settings. A 32.768-KHz crystal is used to clock and update the time and date. The RTC has system wakeup capability for resume on alarm, including Wake on Day-of-Month capability (ACPI and OnNow requirement). This alarm can be programmed with SETUP to wake up the system from standby and suspend-to-RAM states.

The PIIX4 has 256 bytes of battery-backed CMOS memory. The first 128 bytes are the standard CMOS locations, of which the first 14 are used for clock and calendar control. The second 128 bytes can be used for extended CMOS functions.

Read Only Memory (ROM)

The System Power Management, Video BIOS, and the setup program reside in Read only Memory (ROM). The ROM is implemented using one 4-Mbit (512 K × 8 bit) Intel 28F004BV boot block FLASH EPROM device. The flash consists of a 16 -KB boot block section, two 8-K parameter sections, and 480 K of the main section. The 16-KB boot block section stores the initial POST routines. The two 8-K parameter sections are not used. The main 480 K holds the remainder of the code. Normal BIOS upgrades will only update the 480 K main section.

Implementing the BIOS ROM using FLASH technology allows the ROM to be reprogrammed dynamically by a FLASH update program. The FLASH update utility is supplied by Phoenix Technologies (suppliers of the system BIOS). The utility verifies that AC power is applied to the unit and that no memory management drivers are loaded before reprogramming the BIOS. If a failure occurs during the reprogramming (AC power is lost and the main battery is dead), the computer becomes inoperable and the FLASH ROM will have to be crisis-recovered.

Twelve volts is needed for erasing and programming the ROM. One hardware signal is used to program the ROM, FLASHVPPON, since the write protect pin is strapped high and BOOTVPPON can never be used. FLASHVPPON enables 12 volts to the ROM VPP pin and allows the 480-K main section and the two 8-K parameter sections to be programmed. FLASHVPPON is generated by the Super IO.

NOTE: We never use the Boot block feature. Boot block is programmed in the same way as the rest of the block. Compaq uses 2K code in the Super IO; therefore, the Boot block feature can be disabled.

Refer to the *Maintenance and Service Guide* for instructions on how to re-flash the system BIOS.

Super I/O Controller

The Super I/O Controller device is the SMC FDC37N97 (MSIO). It integrates a new generation of complete Super I/O functions, plus an enhanced 8051 microcontroller for power management and keyboard control. The MSIO resides on the SUB-ISA bus and includes the following features:

- 3.3-volt operation with 5-volt tolerant buffers
- ACPI 1.0 and PC99-compliant
- Three power planes
- ACPI embedded controller interface
- Low standby current in sleep mode
- Configuration Register Set compatible with ISA Plug-and-Play standard (version 1.0a)
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- Diskette interface on parallel port
- 8051 controller using parallel port to reprogram the flash ROM
- Advanced infrared communications controller (IrCC 2.0)
- 512-kbyte flash ROM interface
- ISA Host interface with clock run support and ACPI SCI interface
- High-performance embedded 8051 keyboard and system controller
- Four independent hardware-driven PS/2 ports
- Intelligent Auto Power Management
- 1.44-MB Super I/O diskette controller
- IEEE 1284-compliant parallel port with EPP and ECP support
- Shared ROM interface so that the external 8051 Flash ROM can be shared with system BIOS and SM firmware

For more detailed information about the MSIO, refer to Chapter 5.

Clocks

Clock Synthesizer and Clock Buffer

The clock synthesizer and SDRAM clock buffer are CK100-SM compliant components.

The clock generator provides the clocks and low-skew distribution buffers required to drive the Pentium II Processor, 440BX, SDRAM memory, PCI buses, ISA bus and USB. A 14.381 MHz clock crystal provides the reference clock for an internal PLL that generates all other frequencies. The device is operated at a +3.3-volt core voltage with the outputs being at +2.5 volts and +3.3 volts.

The frequency synthesizer operates in a spread spectrum mode to help reduce EMI emissions. Three buffered 14.381-MHz clock outputs are available. These clocks are used by other components in the system such as the MSIO, Maestro 2E, and PIIX4. It provides two copies of CPU clock, five copies of PCI clock, one copy of free running PCI clock, one copy of Ref. Clock at 14.318 MHz. One copy of 48 MHz is used by the USB controller and power management control input pins.

A single input pin is used to select between 66 MHz and 100 MHz for the CPU clock. This pin is strapped to the correct position on the MMC2. The other clocks generated by the clock generator are affected by the CPU clock speed. A 32-KHz clock source is provided by the PIIX4. This 32 KHz-clock is used for refreshing the video memory and system DRAM during standby operation.

Real-Time Clock

The PIIX4M uses a crystal-controlled 32.768-KHz clock to generate the timing signals for its internal real-time clock (RTC). The use of a dedicated crystal oscillator guarantees that the RTC runs smoothly during instances where the system is fully powered off while drawing extremely low current.

Audio Clocks

The Maestro 2E uses a 49.152-MHz crystal to generate its internal timing signals for audio data sampling and conversion rates.

chapter 3

SYSTEM MEMORY

The memory subsystem consists of 32 or 64 MB of 66-MHz (Armada PII) or 64 MB of 100-MHz (Armada PIII) SDRAM. Memory is expandable to 512 MB.

Base System Memory

Both the Armada E500 and Armada V300 computer models support two SODIMM slots and no soldered base memory. One bank will be filled with 32 MB or 64 MB with a 64 bit data path, dependent on the type of computer. The type of memory used must meet the following specifications:

Table 3-1
Memory Specifications

Specification	Type
Type	Synchronous DRAM (SDRAM)
Voltage	3.3 V
Speed	66 MHz (P-II); 100 MHz (P-III)
Refresh	Self-Refresh (128 mS)
Parity	Not supported

System Memory Expansion

Memory expansion is available through the two DIMM sockets. The DIMMs supported are 144-pin 3.3 volt SO-DIMM. The largest SO-DIMM available is 256 MB. This means that the maximum system memory is 256 MB + 256 MB = 512 MB for Pentium II and Pentium III Processors systems.

The system memory is expandable from the base of 32 MB to a total of 512 MB using a combination of 32 MB, 64 MB, 128 MB, and 256 MB memory expansion modules. The following table illustrates the various memory configurations.

Table 3-2
Memory Configurations

Exp. Module (Bank 1)	Exp. Module (Bank 2)	Total Memory
32 MB	32 MB	64 MB
32 MB	64 MB	96 MB
32 MB	128 MB	160 MB
32 MB	256 MB	288 MB
64 MB	64 MB	128 MB
64 MB	128 MB	192 MB
64 MB	256 MB	320 MB
128 MB	128 MB	256 MB
128 MB	256 MB	384 MB
256 MB	256 MB	512 MB

NOTE: The two DRAM banks are interchangeable for the purposes of memory expansion. The table shows the progression of adding memory as System ⇒ Bank 1 ⇒ Bank 2, but the opposite progression (System ⇒ Bank 2 ⇒ Bank 1) is also valid.

chapter 4

PC CARD INTERFACE

The PC Card interface provides system expansion that is transparent to the user through the PC Card slot connectors. The Armada E500 supports two card slots and the Armada V300 supports one slot. Peripherals in the form of PC Cards can be added to the system. The system automatically interrogates the PC Card on insertion to determine its function and requirements. This can be accomplished without powering down, reconfiguring, and restarting the system.

Functional Description

The PC Card interface facilitates the expansion of memory, mass storage, audio/video, and communications capabilities of the computer through easily installable PC Cards.

A functional PC Card interface involves the use of the following components:

- Hardware: The PC Card and the PC Card controller
- Software: A set of special BIOS calls, routines, and device drivers that mediate between the hardware, operating system, and application software. Compaq products are provided with multilayered software support for PC Card operation. PC cards may also require and come with device drivers to facilitate interface support.

CardBus Controller

The Texas Instruments PCI1225 is a high-performance PCI-to-PC Card controller with a 32-bit PCI interface. The device supports two independent PC Card sockets compliant with the 1997 PC Card Standard and the PCI Bus Interface Specification for PCI-to-CardBus bridges. The Armada E500 can use both of these slots but the Armada V300 uses only one. The PCI1225 supports any combination of 16-bit and CardBus PC Cards in the two sockets, powered at 5 VDC or 3.3 VDC, as required.

The PCI1225 is compliant with the latest PCI Bus Power Management Specification. It is also compliant with the PCI Local Bus Specification revision 2.1, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers, or CardBus PC Card bridging transactions.

All card signals are internally buffered to allow hot insertion and removal. The PCI1225 is register-compatible with the Intel 82365SL-DF ExCA controller. The PCI1225 internal data-path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-

bit PCI cycles. The PCI1225 can also be programmed to accept fast posted writes to improve system bus usage.

The PCI1225 provides an externally buffered Zoomed Video (ZV) path. Multiple system interrupt signaling options are provided: Serial ISA/Serial PCI, Serial ISA/Parallel PCI, Parallel ISA/Parallel PCI, and PCI Only interrupts. Furthermore, general-purpose inputs and outputs (GPIOs) are provided to implement sideband functions.

An advanced complementary metal-oxide semiconductor (CMOS) process achieves low system power consumption while operating at PCI clock rates of up to 33 MHz. Several low-power modes allow the host power management system to further reduce power consumption.

A list of general features includes the following:

- Zoomed VideoCard
- Zoomed Video auto-detect
- 3.3-volt core logic with universal PCI interfaces compatible with 3.3-volt and 5-volt PCI signaling environments
- Mix-and-match 5-volt/3.3-volt PC cards and 3.3-volt CardBus cards
- Support for two PC card or CardBus slots with hot insertion and removal with the Armada E500; only one slot used with the Armada V300
- Serial interface to TI TPS2206 dual power switch
- Support for 132 Mbyte/s burst transfers to maximize data throughput on both the PCI bus and the CardBus bus
- Support for serialized IRQ with PCI interrupts
- Eight-way Legacy IRQ multiplexing
- Support for interrupt modes: Serial ISA/Serial PCI, Serial ISA/Parallel PCI, Parallel ISA/Parallel PCI, Parallel PCI only
- Four general purpose I/Os
- Supports distributed DMA and PC/PCI DMA
- Supports 16-bit DMA on both PC card sockets
- Supports Ring Indicate, SUSPEND, and PCI CLKRUN
- Advanced submicron, low-power CMOS technology
- VGA/palette memory and I/O; subtractive decoding options

System Block Diagram

Figure 4-1 shows a simplified system implementation using the PCI1225. The PCI interface includes all address/data and control signals for PCI protocol. Highlighted in this diagram is the functionality supported by the PCI1225. The PCI1225 supports PC/PCI DMA, PCI Way DMA (distributed DMA), PME wake-up from D3 through D0, 4 interrupt modes, a Zoomed Video port, and 12 multifunction pins (8 IRQMUX, and 4 GPIO pins) that can be programmed for a wide variety of functions.

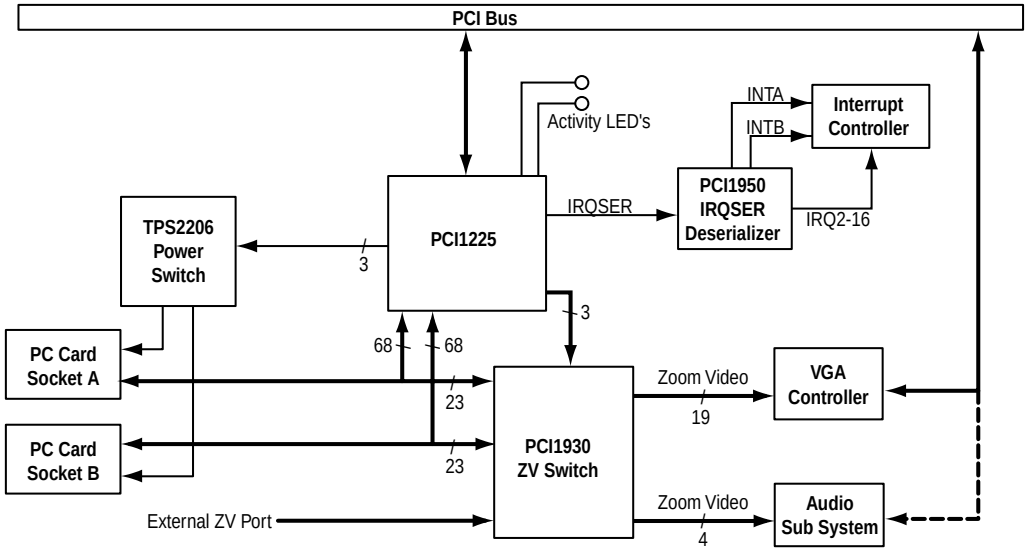

Figure 4-1. *PCI1225 Simplified System Block Diagram*

Clamping Rail Splits

The I/O sites can be pulled through a clamping diode to a power rail for protection. The core power supply is independent of the clamping rails. The clamping (protection) diodes are required if the signaling environment on an I/O is system-dependent. For example, PCI signaling can be either 3.3 VDC or 5.0 VDC, and the PCI1225 must reliably accommodate both voltage levels. This is accomplished by using a 3.3 volt buffer with tolerance (protection) at V_{CCP} .

PCI Interface

This section describes the PCI interface of the PCI1225, and how the device responds and participates in PCI bus cycles. The PCI1225 provides all required signals for PCI master/slave devices.

PCI Bus Lock

The bus locking protocol defined in the PCI Specification is not highly recommended, but is provided on the PCI1225 as an additional compatibility feature. The PCI LOCK* terminal is multiplexed with GPIO2, and the terminal function defaults to a general-purpose input (GPI). The use of LOCK* is only supported by PCI-to-CardBus bridges in the downstream direction (away from the processor).

PCI LOCK* indicates an atomic operation that may require multiple transactions to complete. When LOCK* is asserted, nonexclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on the PCI bus does not guarantee control of LOCK*; control of LOCK* is obtained under its own protocol. It is possible for different initiators to use the PCI bus while a single master retains ownership of LOCK*. To avoid confusion with the PCI bus clock, the CardBus signal for this protocol is CBLOCK*.

An agent may need to do an exclusive operation because a critical memory access might be broken into several transactions, but the master wants exclusive rights to a region of memory. The granularity of the lock is defined by PCI to be 16 bytes aligned. The lock protocol defined by PCI allows a resource lock without interfering with nonexclusive, real-time data transfer, such as video.

The PCI bus arbiter can be designed to support only complete bus locks using the LOCK* protocol. In this scenario, the arbiter will not grant the bus to any other agent (other than the LOCK* master) while LOCK* is asserted. A complete bus lock can have a significant impact on the performance of the video. The arbiter that supports complete bus lock must grant the bus to the cache to perform a writeback due to a snoop to a modified line when a locked operation is in progress.

The PCI1225 supports all LOCK* protocol associated with PCI-to-PCI bridges and PCI-to-CardBus bridges. This includes disabling write posting while a locked operation is in progress, which can solve a potential deadlock when using devices such as PCI-to-PCI bridges. The potential deadlock can occur if a CardBus target supports delayed transactions and blocks access as the target until it completes a delayed read. This target characteristic is prohibited by the 2.1 PCI Specification, and the issue is resolved by the PCI master using LOCK*.

PC Card Applications Overview

This section describes the PC Card interfaces of the PCI1225. A discussion is provided on PC Card recognition, which details the card interrogation procedure. The card powering procedure is discussed, including the protocol of the P2C power switch interface. The ZV buffering provided by the PCI1225 and programming model is also detailed in this section.

PC Card Insertion, Removal, and Recognition

The 1995 PC Card Standard addresses the card detection and recognition process through an interrogation procedure that the socket must initiate upon card insertion into a cold, unpowered socket. Through this interrogation, card voltage requirements and interface (16-bit versus CardBus) are determined.

The scheme uses the CD1, CD2, VS1, and VS2 signals (CCD1, CCD2, CVS1, CVS2 for CardBus). These four pins are connected in a certain configuration depending on the type of card and the supply voltage.

P2C Power Switch Interface (TPS2206)

A power switch with a PCMCIA-to-peripheral control (P2C) interface is required for the PC Card powering interface. The TI TPS2206 Dual-Slot PC Card power-interface switch provides the P2C interface to the CLOCK, DATA, and LATCH terminals of the PCI1225.

Zoomed Video Support

The Zoomed Video (ZV) port on the PCI1225 provides an externally buffered 16-bit ZV PC Card data path. This internal routing is programmed through the multimedia control register.

The PCI1225 defaults to socket 0 (see the multimedia control register). When ZVOUTEN is enabled, the Zoomed Video output terminals are enabled and allow the PCI1225 to route the Zoomed Video data. However, no data is transmitted unless either ZVEN0 or ZVEN1 is enabled in the multimedia control register. If the PORTSEL maps to a card port that is disabled (ZVEN =0 or ZVEN1 = 0), the Zoomed Video port is driven low (for example, no data is transmitted).

D3_STAT* Pin

An additional feature of the 1225 is the D3_STAT* (D3 status) pin. This pin is asserted under the following two conditions. Both conditions must be true before D3_STAT* is asserted.

- Function 0 and Function 1 are placed in D3.
- PME* is enabled.

The intent of including this feature in the PCI1225 is to use this pin to switch an external V_{CC} /V_{AUX} switch. This feature can be programmed on GPIO1 pin (terminal W11) by writing 01b to bits 7–6 of the GPIO1 control register (PCI offset 89h).

Internal Ring Oscillator

The internal ring oscillator provides an internal clock source for the PCI1225 so that neither the PCI clock nor an external clock is required for the PCI1225 to power down a socket or interrogate a PC Card. This internal oscillator operates nominally at 16 KHz and can be enabled by setting bit 27 of the system control register (PCI offset 80h) to a 1b. This function is disabled by default.

SPKROUT Usage

The SPKROUT signal carries the digital audio signal from the PC Card to the system. When a 16-bit PC Card is configured for I/O mode, the BVD2 pin becomes SPKR*. This terminal, also used in CardBus applications, is referred to as CAUDIO. SPKR* passes a TTL level digital audio signal to the PCI1225. The CardBus CAUDIO signal also can pass a single amplitude, binary waveform. The binary audio signals from the two PC Card sockets are XORed in the PCI1225 to produce SPKROUT. Figure 4-2 illustrates the SPKROUT connection.

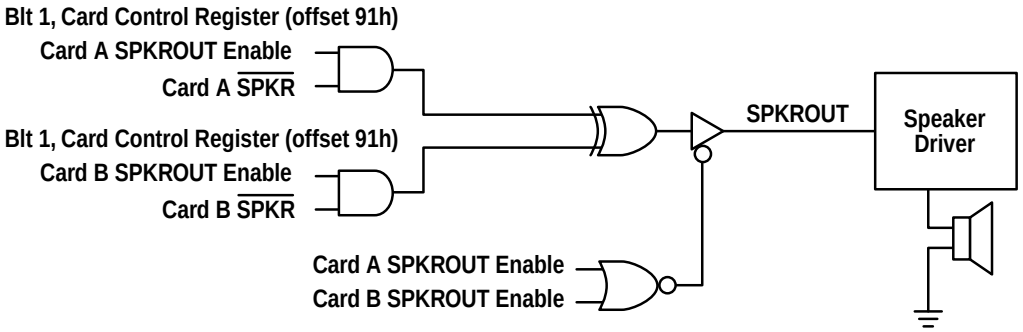

Figure 4-2. *SPKROUT Connection to Speaker Driver*

The SPKROUT signal is typically driven only by PC modem cards. The PCI1130/1131 requires a pull-up resistor on the SUSPEND/SPKROUT terminal. Because the PCI1225 does not multiplex any other function on SPKROUT, this terminal does not require a pull-up resistor.

PC Card 16 DMA Support

The PCI1225 supports both PC/PCI (centralized) DMA and a distributed DMA slave engine for 16-bit PC Card DMA support. The distributed DMA (DDMA) slave register set provides the programmability necessary for the slave DDMA engine.

Programmable Interrupt Subsystem

Interrupts provide a way for I/O devices to let the microprocessor know that they require servicing. The dynamic nature of PC Cards and the abundance of PC Card I/O applications require substantial interrupt support from the PCI1225. The PCI1225 provides several interrupt signaling schemes to accommodate the needs of a variety of platforms. The different mechanisms for dealing with interrupts in this device are based on various specifications and industry standards. The ExCA register set provides interrupt control for some 16-bit PC Card functions, and the CardBus socket register set provides interrupt control for the CardBus PC Card functions. The PCI1225 is therefore backward-compatible with existing interrupt control register definitions, and new registers have been defined where required.

The PCI1225 detects PC Card interrupts and events at the PC Card interface and notifies the host controller through one of several interrupt signaling protocols. To simplify the discussion of interrupts in the PCI1225, PC Card interrupts are classified as either card status change (CSC) or as functional interrupts.

The method by which any type of PCI1225 interrupt is communicated to the host interrupt controller varies from system to system. The PCI1225 offers system designers the choice of using parallel PCI interrupt signaling, parallel ISA type IRQ interrupt signaling, or the IRQSER serialized ISA and/or PCI interrupt protocol. Traditional ISA IRQ signaling is provided through eight IRQMUX terminals. It is possible to use the parallel PCI interrupts in combination with either parallel IRQs or serialized IRQs, as detailed in the sections that follow.

PC Card Functional and Card Status Change Interrupts

PC Card functional interrupts are defined as requests from a PC Card application for interrupt service. They are indicated by asserting specially defined signals on the PC Card interface. Functional interrupts are generated by 16-bit I/O PC Cards and by CardBus PC Cards.

Card status change (CSC) type interrupts are defined as events at the PC Card interface that are detected by the PCI1225 and may warrant notification of host card and socket services software for service. CSC events include both card insertion and removal from PC Card sockets, as well as transitions of certain PC Card signals.

CSC and functional interrupt sources are dependent on the type of card inserted in the PC Card socket. The three types of cards that may be inserted into any PC Card socket are: 16-bit memory card, 16-bit I/O card, and CardBus cards. Functional interrupt events are valid only for 16-bit I/O and CardBus cards; that is, they are not valid for 16-bit memory cards. Card insertion and removal type CSC interrupts are independent of the card type.

The signal naming convention for PC Card signals describes the function for 16-bit memory and I/O cards, as well as CardBus. For example, the READY(IREQ*)//CINT* signal includes the READY signal for 16-bit memory cards, the IREQ* signal for 16-bit I/O cards, and the CINT* signal for CardBus cards. The 16-bit memory card signal name is first, with the I/O card signal name second enclosed in parentheses. The CardBus signal name follows after a forward double slash (//).

The PC Card standard describes the power-up sequence that must be followed by the PCI1225 when an insertion event occurs and the host requests that the socket V_{CC} and V_{PP} be powered. On completion of this power-up sequence, the PCI1225 interrupt scheme may be used to notify the host system, denoted by the power cycle complete event. This interrupt source is considered a PCI1225 internal event because it does not depend on a signal change at the PC Card interface, but rather the completion of applying power to the socket.

Interrupt Masks And Flags

Host software may individually mask or disable most of the potential interrupt sources by setting the appropriate bits in the PCI1225. By individually masking the interrupt sources, software can control which events will cause a PCI1225 interrupt. Host software has some control over which system interrupt the PCI1225 will assert by programming the appropriate routing registers. The PCI1225 allows host software to route PC Card CSC and PC Card functional interrupts to separate system interrupts.

When an interrupt is signaled by the PCI1225, the interrupt service routine must be able to discern what kind of event caused the interrupt. Internal registers in the PCI1225 provide flags that report which interrupt source was the cause of an interrupt. By reading these status bits, the interrupt service routine can determine which action should be taken. All interrupts may be masked except the functional PC Card interrupts, and an interrupt status flag is available for all types of interrupts.

There is not a mask bit to stop the PCI1225 from passing PC Card functional interrupts through to the appropriate interrupt scheme. Functional interrupts should not be fired until the PC Card is initialized and powered.

The flag bits in the ExCA registers (16-bit PC Card-related interrupt flags) may be cleared by two different methods. One method is an explicit write of 1 to the flag bit to clear, and the other is a reading of the flag bit register. The selection of flag bit clearing is made by bit 2 in the global control register (ExCA offset 1Eh/5Eh/81Eh), and defaults to the flag are cleared on read method.

The CardBus-related interrupt flags can only be cleared by an explicit write of 1 to the interrupt flag in the socket event register. Although some of the functionality is shared between the CardBus registers and the ExCA registers, software should not program the chip through both register sets when a CardBus card is functioning.

Legacy Interrupt Multiplexer

The IRQ multiplexer implemented in the PCI1225 provides a mechanism to route the IRQMUX signals to any of the 15 legacy IRQ signals. The IRQMUX7–6 signals share the PC/PCI DMA terminals, and take precedence when routed. The other six IRQMUX signals (IRQMUX5–IRQMUX0) are available in all platforms. To use the IRQMUX interrupt signaling, software must program the device control register, located at PCI offset 92h, to select the legacy IRQ signaling scheme.

Figure 4-3 illustrates the IRQMUX functionality. This illustration describes only the PCREQ/IRQMUX7/SCL signal.

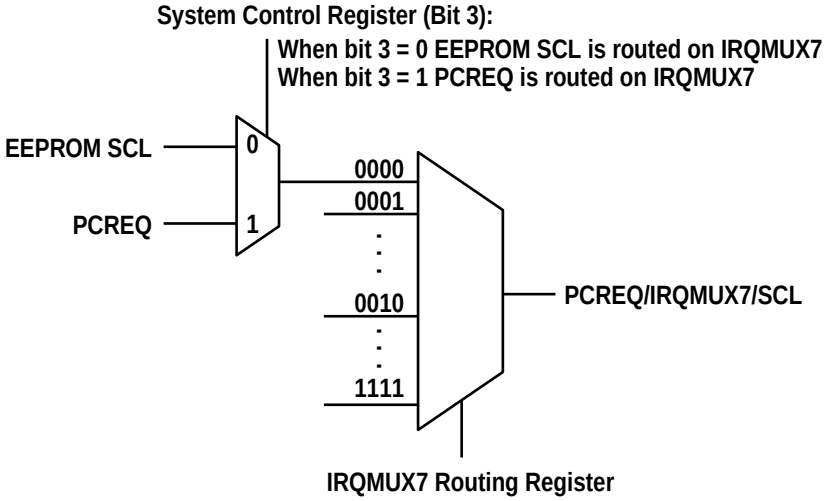

Figure 4-3. *Interrupt MUX Functionality - Example of IRQMUX7 Routing*

If parallel ISA IRQs are selected in the device control register, then the IRQMUX routing register, located at PCI offset 8Ch, must be programmed with the associated ISA IRQ connections. The PCI1225 supports up to eight parallel ISA IRQ signal connections, IRQMUX7–IRQMUX0.

Figure 4-4 is an example PCI1225 IRQ implementation that provides eight ISA interrupts.

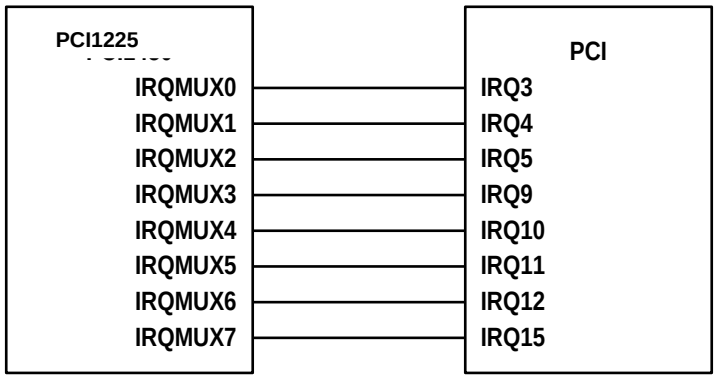

Figure 4-4. *Example PCI1225 IRQ Implementation*

The system in the preceding example cannot support PC/PCI DMA because all eight ISA IRQs are used. In this example, the IRQMUX7 and IRQMUX6 terminals are used to signal ISA IRQs, and are not available for PC/PCI DMA. For systems not using all eight IRQs, PC/PCI DMA can be implemented and coexist with ISA IRQs by using IRQMUX6 and IRQMUX7 for PC/PCI DMA. For instance, legacy IRQs and PC/PCI DMA implementation are not mutually exclusive. However, if the IRQMUX registers are programmed to use IRQMUX7–IRQMUX6, they will override PC/PCI DMA.

Software is responsible for programming the IRQMUX routing register to reflect the IRQ configuration shown in Figure 4-4. In this example, this programming is accomplished by writing a double-word of data FCBA9543h to the PCI1225 IRQMUX routing register, PCI offset 8Ch. In this example (FCBA9543h), F corresponds to

IRQ15, C to IRQ12, B to IRQ11, A to IRQ10, 9 to IRQ9, 5 to IRQ5, 4 to IRQ4, and 3 to IRQ3.

The IRQMUX routing register is shared between the two PCI1225 functions, and only one write to function 0 or function 1 is necessary to configure the IRQMUX signals.

Using Parallel PCI Interrupts

Parallel PCI interrupts are available when in pure parallel PCI interrupt mode, IRQMUX signaling mode, and when only IRQs are serialized with the IRQSER protocol. The PCI interrupt signaling is dependent on the interrupt mode. The interrupt mode is selected in the device control register (92h). The IRQSER/INTB* signals INTB when one of the parallel interrupt modes is selected through bits 2–1 in the device control register (92h). PCI INTB* is also available on the IRQMUX0 terminal by programming bits 3–0 to 0001b in the IRQMUX routing register (8Ch). PCI INTA* is available on the GPIO3 terminal by programming bits 7–6 in the GPIO3 control register.

Power Management Overview

In addition to the low-power CMOS technology process used for the PCI1225, various features are designed into the device to allow implementation of popular power saving techniques. These features and techniques are discussed in this section.

CLKRUN* Protocol

CLKRUN* is the primary method of power management on the PCI bus side of the PCI1225. Because some chipsets do not implement CLKRUN*, this is not always available to the system designer so alternate power savings features are provided.

If CLKRUN* is not implemented, the CLKRUN* pin should be tied low. CLKRUN* is enabled by default through bit 1 (KEEPCLK) in the system control register (80h).

CardBus PC Card Power Management

The PCI1225 implements its own card power management engine that can turn off the CCLK to a socket when there is no activity to the CardBus PC Card. The CCLK can also be configured as divide by 16 instead of stopped. The CLKRUN* protocol is followed on the CardBus interface to control this clock management.

CardBus Device Class Power Management

The specific issues addressed by the PCI Bus Interface Specification for PCI-to-CardBus bridges for D3 wake-up are:

- Preservation of device context: The PCI Power Management Specification version 1.0 states that PRST* must be asserted when transitioning from $D3_{cold}$ to D0. A method to preserve wake-up context must be implemented so that PRST* does not clear the PME* context registers.
- Power source in $D3_{cold}$ if wake-up support is required from this state.

The PCI1225 addresses these D3 wake-up issues as follows:

- Preservation of device context: When PRST* is asserted, bits required to preserve PME* context are not cleared. To clear all bits in the PCI1225, another reset pin is defined: G_RST* (global reset). G_RST* is normally only asserted during the initial power-on sequence. After the initial boot, PRST should be asserted so that PME context is retained for D3-to-D0 transitions. Bits cleared by G_RST*, but not cleared by PRST* (if the PME* enable bit is set), are referred to as PME* context bits.
- Power source in $D3_{cold}$ if wake-up support is required from this state. Because V_{CC} is removed in $D3_{cold}$, an auxiliary power source must be switched to the PCI1225 V_{CC} pins. This switch should be a make before break type of switch, so that V_{CC} to the PCI1225 is not interrupted.

Master List of PME* Context Bits and Global Reset-Only Bits

PME* context bit means that the bit is cleared only by the assertion of G_RST* when the PME* enable bit is set (PCI offset A4h, bit 8). If PME* is not enabled, these bits are cleared when either PRST* or G_RST* is asserted.

Global reset-only bits, as the name implies, are only cleared by G_RST*. These bits are never cleared by PRST*, regardless of the setting of the PME* enable bit (PCI offset A4h, bit 8). The G_RST* signal is gated only by the SUSPEND* signal. This means that assertion of SUSPEND* blocks the G_RST* signal internally, thereby preserving all register contents.

Suspend mode

The SUSPEND* signal, provided for backward compatibility, gates the PRST* (PCI reset) signal and the G_RST* (global reset) signal from the PCI1225. Besides gating PRST* and G_RST*, SUSPEND* also gates PCLK inside the PCI1225 to minimize power consumption.

Gating PCLK does not create any issues with respect to the power switch interface in the PCI1225. This is because the PCI1225 does not depend on the PCI clock to clock the power switch interface.

There are two methods to clock the power switch interface in the PCI1225:

- Use an external clock to the PCI1225 CLOCK pin
- Use the internal oscillator

Asynchronous signals, such as card status change interrupts and RI_OUT, can be passed to the host system without a PCI clock. However, if card status change interrupts are routed over the serial interrupt stream, the PCI clock will have to be restarted to pass the interrupt because neither the internal oscillator nor an external clock is routed to the serial interrupt state machine.

Requirements for SUSPEND*

A requirement for implementing suspend mode is that the PCI bus must not be parked on the PCI1225 when SUSPEND* is asserted. The PCI1225 responds to SUSPEND* being asserted by tri-stating the REQ* pin. The PCI1225 will also gate the internal clock and reset.

The GPIOs, IRQMUX signals, and RI_OUT* signals are all active during SUSPEND*, unless they are disabled in the appropriate PCI1225 registers.

Ring Indicate

The RI_OUT* output is an important feature used in legacy power management. It is used to enable a system to go into a suspended mode and wake up on modem rings and other card events.

The RI_OUT* signal on the PCI1225 can be asserted under any of the following conditions:

- A 16-bit PC Card modem in a powered socket asserts RI* to indicate an incoming call to the system.
- A powered down CardBus card asserts CSTSCHG (CBWAKE), requesting system and interface wake up.
- A card status change (CSC) event, such as insertion or removal of cards, battery voltage levels, occurs.

A CSTSCHG signal from a powered CardBus card is indicated as a CSC event, not as a CBWAKE event. These two RI_OUT* events are enabled separately. Figure 4-5 details various enable bits for the PCI1225 RI_OUT* function; however, it does not illustrate the masking of CSC events. See interrupt masks and flags for further description of CSC interrupt masks and flags.

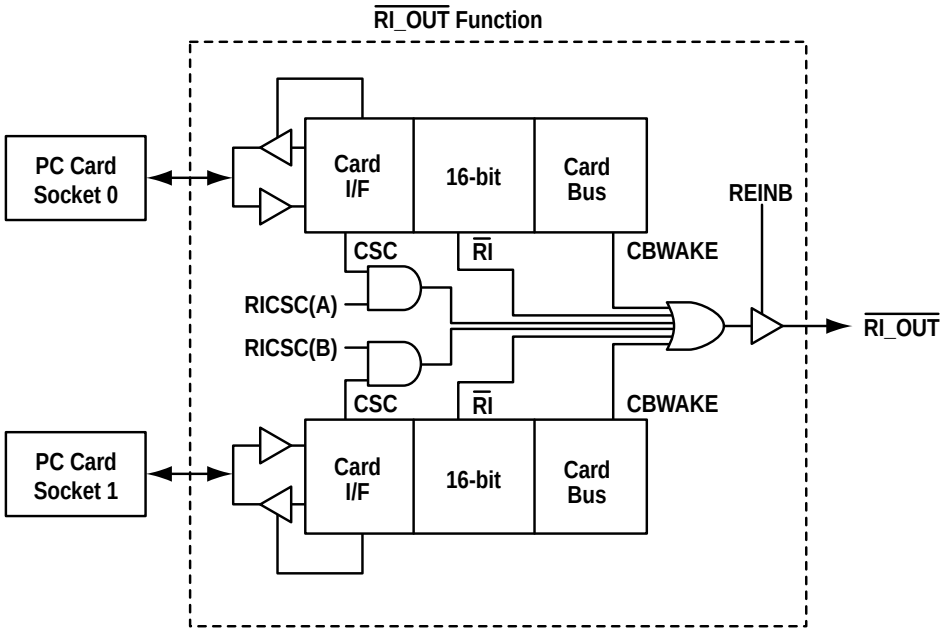

Figure 4-5. *RI_OUT* Functional Block Diagram*

RI_OUT* is multiplexed on the same pin with PME*. The default is for RI_OUT* to be signaled on this pin. In PCI power managed systems, the PME* signal should be enabled by setting bit 0 (RI_OUT*/PME*) in the system control register (80h) and clearing bit 7 (RIENB) in the card control register (91h).

Routing CSC events to the RI_OUT* signal, enabled on a per socket basis, is programmed by the RICSC bit in the card control register. This bit is socket-dependent (not shared).

The RI* signal from the 16-bit PC Card interface is masked by the ExCA control bit RINGEN in the ExCA interrupt and general control register. This is programmed on a per socket basis, and is only applicable when a 16-bit card is powered in the socket.

The CBWAKE signaling to RI_OUT* is enabled through the same mask as the CSC event for CSTSCHG. The mask bit, CSTSMASK, is programmed through the socket mask register in the CardBus socket registers.

chapter 5

SUPER I/O CONTROLLER

The FDC37N97X MSIO Super I/O Controller used in the Armada E500 and Armada V300 computers is made by SMC. It integrates a new generation of complete Super I/O functions, plus provides an enhanced 8051 microcontroller for power management and keyboard control. The main features of this device are:

- The FDC37N971 incorporates a high performance 8051-based keyboard controller, 2 kB of internal ROM and 256 bytes of RAM; a 512-kB Flash ROM interface; support for four PS/2-type pointing device/keyboard interfaces; a real-time clock; two I^2C controllers, and GPIOs
- Implementation of full ACPI compliant embedded controller interface
- Diskette controller with advanced digital data separator and 16-byte data FIFO; an NS16C550A-compatible UART, SMSC's advanced Infared Communications Controller (IrCC 2.0) with a UART and a Synchronous Communications Engine to provide IrDa v1.1 (Fast IR) capabilities
- IEEE 1284-compliant parallel port with EPP and ECP support; a serial IRQ peripheral agent interface; two independently programmable pulse width modulators; two-diskette direct drive support
- Shared ROM interface so that the external 8051 Flash ROM can be shared with system BIOS and SM firmware

The enhanced 8051 performs all keyboard related functions, including those normally handled by an 8042. As shown in Figure 5-1, the system processor communicates with the keyboard and other auxiliary devices through ports 60h (data) and 64h (status). In addition, the Compaq-specific functions that support power management, popups, keyboard to system processor interface, and mouse input are embedded in the system logic. The MSIO functions are described in the following sections.

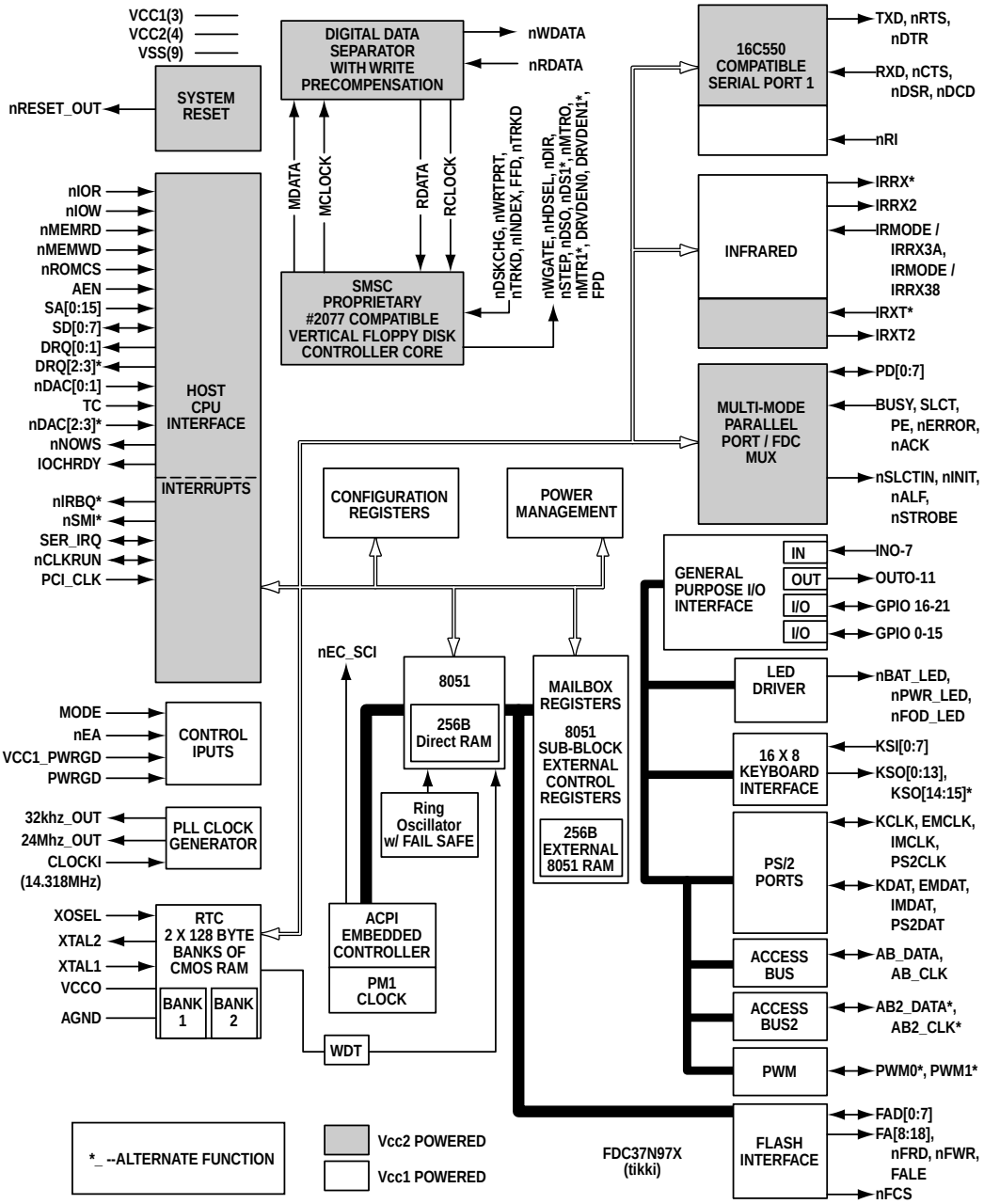

Figure 5-1. *SMC FDC37N97X MSIO Super I/O Controller*

8051 Microcontroller

The MSIO device integrated a high performance 8051 embedded controller compatible with the industry standard 80C51 microcontroller. The high performance 8051 features include:

- Keyboard controller providing 2 kB of internal ROM, 256 bytes of RAM; a 512 KB of Flash ROM interface; support four PS/2-type pointing device/keyboard interfaces; a real-time clock; two I^2C controllers; and GPIOs
- 2.5X average instruction execution speed improvement over the entire instruction set; for example, typical 4-clock instruction cycle in high-performance 8051 versus 12-clock instruction cycle in standard 8051
- Faster clock speed: 24 MHz or higher versus 16 MHz in standard 8051
- Dual data pointers: (includes new SFR)
- More interrupts: power-fail, external interrupt 2, external interrupt 3, etc.

The host interfaces to the 8051 through mailbox registers, shown in Figure 5-2. The mailbox registers interface (host access ports) are run-time registers that occupy two addresses in the system I/O space. The access ports are used by the host to read and write the 44 registers. Mailbox register 0 is dedicated for system-to-8051 communications. Any write by the system to this address will generate an 8051 interrupt. Mailbox register 1 is dedicated for 8051-to-system communications. Any writes to this register by the 8051 will generate an SMI interrupt (if enabled) to the host. The remaining mailbox registers can be accessed by the system and the 8051 and are used to pass parameters. Firmware must take precautions to avoid simultaneous use of these registers by both 8051 and system.

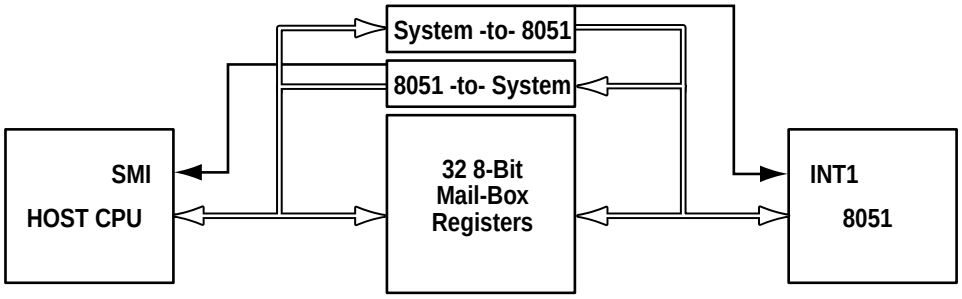

Figure 5-2. *System-to-8051 Mailbox Interface Registers Block Diagram*

Some of the peripherals described below are actually 8051 peripherals, so the host cannot directly access them. For example, to access the GPIO registers, the system must pass the parameters to the 8051 through the mailbox registers, using a scheme defined by the firmware architecture.

The 8051 communicates with the temperature sensors, the EEPROMs, batteries, and docking stations through the I^2C bus. Information obtained from these devices is passed on to the host controller. See the I^2C controller section for more details. The 8051 controls the charging and discharging of the batteries.

Power-On Sequence

The 8051 and its ROM are connected to a separate power rail from the system. This power is provided by a regulator that is operational any time there is a power source (AC adapter, battery, or auxiliary battery). An 8051 OUT pin (Out2, RSMRST#) is used to enable the DC/DC converters through the Southbridge (PXII4M) which controls power to the system.

The following is a basic description of the power-on sequence.

When the 8051 is powered up, it executes from its internal 2 kB ROM code. It will first perform a checksum on the external Flash ROM. If this checksum fails, the 8051 transitions into “Flash Disaster Recovery” mode by flashing the power and battery LEDs and polling the parallel port for connection to an external host. This host can then program the flash with new KBC and BIOS code.

If the Flash checksum is valid, the 8051 executes from the external ROM. This external ROM should complete initialization of the 8051 and wait for the power switch to be depressed. When the switch is pressed, the 8051 turns on the system power by driving the RSMRST#_3 signal (OUT2) active to PXII4M. PXII4# in turn drives the SUSA#_3, SUSB#_3 and SUSC#_3 signals high which turns on the DC/DC converters. After about 100 ms, the DC/DC subsystem asserts PWR_GOOD_3 to the 8051, indicating that the system power is on and stable. The 8051 holds the system in reset by keeping the SYS_RESET#_3 signal active. The 8051 then sets an internal timer, places itself into idle mode, and waits for an interrupt. When the timer expires, SYS_RESET#_3 is driven inactive, the 8051 clock is stopped, and the ROM interface is multiplexed onto the system bus.

At this point, PXII4M samples SYS_RESET#_3 active, indicating that the system is ready to run. PXII4M then releases PCI_RESET#_3, which in turn causes the 443BX to release CPU reset, allowing the CPU to begin executing code. This code is fetched from the shared ROM. Eventually, the code is copied into DRAM, and the 8051 clock is started again by the host. The host can no longer access the shared ROM once this happens, since the 8051 owns the interface and executes from the ROM.

Real-Time Clock and CMOS RAM

The real-time clock (RTC) and CMOS RAM in the MSIO are not utilized in the Armada E500 and Armada V300 computers.

Diskette Controller

The 82077AA-compatible diskette controller (FDC) provides the interface between the computer and the diskette drive. The FDC integrates the functions of the formatter/controller, digital data separator, write precompensation, and data rate selection logic for an IBM XT/AT-compatible FDC. Moreover, the MSIO Super I/O controller implements Write protect function, shown in Figure 5-3.

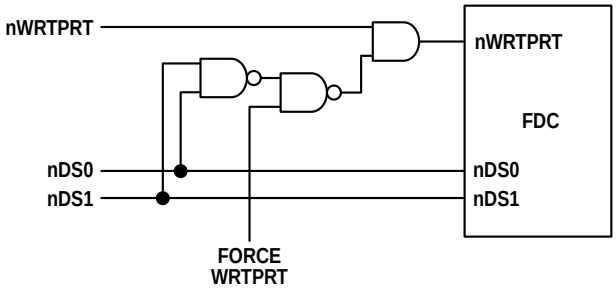

Figure 5-3. *FDC Force Write Protect Function*

Parallel Port

The parallel port, shown in Figure 5-4, is integrated in the MSIO Super I/O device. It supports the optional PS/2 bidirectional parallel port (SPP), the Enhanced Parallel Port (EPP 1.9 and EPP 1.7), and the Extended Capabilities Port (ECP) modes. The parallel port pins are also accessible by the 8051, which allows the 8051 to perform flash recovery through this interface. The diskette controller is also multiplexed to the parallel port, thus providing three-spindle support.

The EPP and ECP modes of operation require a driver to be supplied by the peripheral vendor.

Refer to the SMC 37N97X specification for additional information.

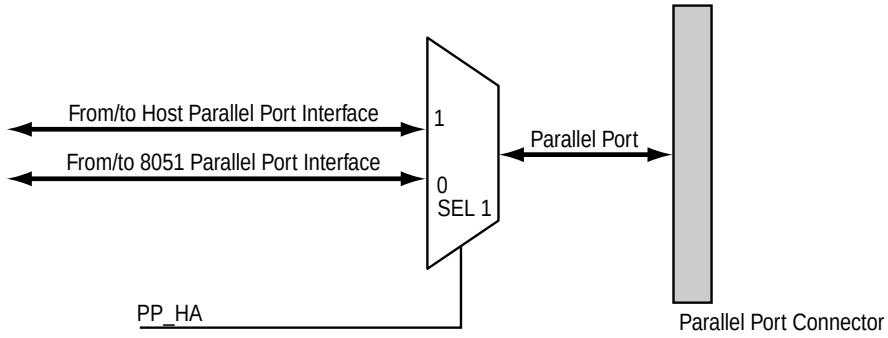

Figure 5-4. *MSIO Parallel Port Multiplexor*

GPIO Usage

The MSIO Super I/O Controller provides eight general-purpose input pins, 12 general purpose-outputs, and 22 general-purpose I/O pins. Improvements on these pins are made for system management flexibility. The GPIO pins, shown in Figure 5-5, are controlled by the 8051, so that host access to them are through the mailbox registers.

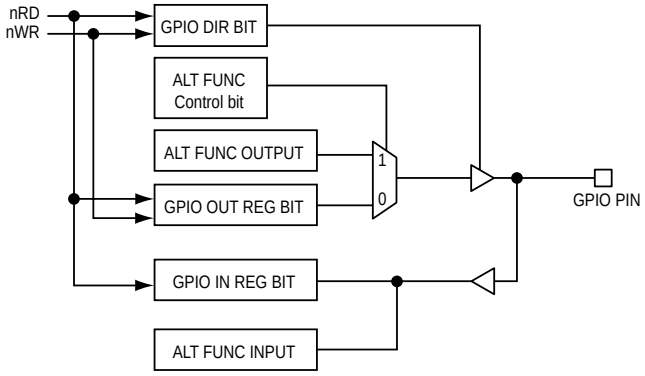

Figure 5-5. *Compaq Armada E500 and Armada V300 MSIO GPIO Pins*

I²C Controller

The new-generation MSIO provides two 8584-compatible I^2C serial data bus controllers. This device is connected to the 8051 internally, so all host access must be through the mailbox structure. The primary I^2C bus is for battery communication and docking control, and the second I^2C bus is for thermal sensor control and EEPROM reading, primarily by the 8051 power management controller.

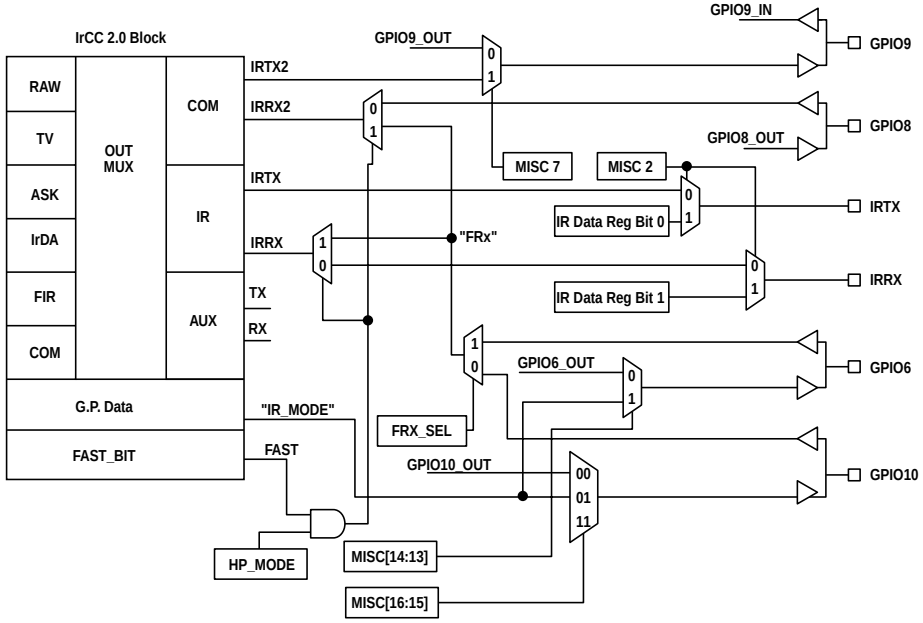

Figure 5-6. *MSIO Infrared Controller Logic*

Serial UARTs

Two 16550A-compatible UARTS are provided in the MSIO. They can be mapped to any of the standard legacy I/O addresses and interrupts. UART-A is dedicated to the RS-232 transceiver and serial connector on the back of the unit. UART-B interfaces internally to an IrDA-compliant infrared encode/decoder and an IrDA module for serial infrared communications. Information on configuration of the UARTs can be found in the MSIO documentation.

Shared Flash ROM Interface

The MSIO provides a means for the system processor to access the 8051 ROM, so that a single Flash ROM device, shown in Figure 5-7, can be used to store system BIOS as well as 8051 code. To prevent simultaneous access by both processors, the 8051 enters the idle mode and stops its internal clock when the reset-out line (SYS_RESET#_3) is deasserted by the 8051 to PXII4M. The system CPU then has control of the ROM interface and "boots" from the ROM. After executing some very basic test routines, the BIOS code copies itself into system DRAM, begins to execute from DRAM, then starts the 8051 clock again. The system does not need to access the ROM again until it loses power to the DRAM.

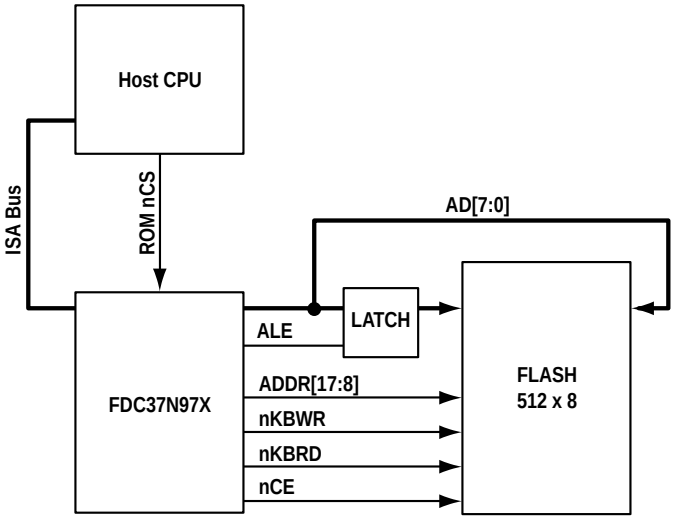

Figure 5-7. *MSIO Flash ROM Interface Block Diagram*

Because the SMC FDC37N97X operates at a higher frequency (24 MHz) compared to the previous 951, the Flash ROM access speed needs to be higher. As it is easier to obtain high speed Flash ROMs that operate at +5 volts rather than +3.3 volts, the Flash ROMs are powered off +5 V_{CC} while the 97X runs off +3 V_{CC}.

Keyboard Scan

The MSIO provides logic to support a scanned keyboard matrix, with 16 Scan Out (KSO) lines and 8 Scan Input (KSI) lines, supporting up to 128 (16 × 8) separate keys on the matrix. However, the E500 and V300 only use up to 12 Scan Out lines. Any single KSO line can be driven, or all can be driven simultaneously. If all lines are driven active, then the scan logic can generate an interrupt if any of the KSI lines go active. This allows the keyboard controller to wait for a key press without having to repeatedly poll the entire matrix.

PS/2 Serial Mouse/Keyboard Interfaces

The MSIO provides two PS/2 channels to support four PS/2-compatible mouse/keyboard interfaces. All four interfaces can operate simultaneously if supported by 8051 firmware. They are used in the Armada E500 and Armada V300 to support the internal pointing stick or touchpad, an external keyboard, and an external mouse. One of the ports is currently not used.

For these computers, the external mouse and keyboard share the same PS/2 channel in the MSIO. Both interfaces are controlled by the internal 8051 microcontroller. Host access is through port 60h and 64h for 8042 keyboard controller compatibility.

Both interfaces mechanically share the same six-pin PS/2 connector. Nevertheless, both external mouse and keyboard can still be operating simultaneously through a Y-cable on the computer. On the Y-cable, the mouse interface has the pin-outs of 1, 3, 4, and 5, whereas the keyboard interface has pins 2, 3, 4, and 6.

chapter 6

AUDIO SUBSYSTEM

The Armada E500 and Armada V300 computers have an internal, industry-standard audio controller, the Maestro 2E from ESS Technology. It supports 16-bit stereo audio, wavetable synthesis, and four-operator FM music synthesis. The Maestro 2E provides all digital sound creation and reproduction tasks and uses an AC97-compatible CODEC, the ES1921, as its interface to the analog world.

The Maestro 2E can record, compress, and play back voice, sound, and music with built-in mixer controls. It consists of an embedded microprocessor, 16-bit stereo A/D and D/A, 64-voice wavetable synthesizer, 20-voice FM music synthesizer, DMA control, and ISA bus interface logic. The Maestro 2E also takes the PC speaker output and converts it to an analog signal with volume control.

Functional Description

The ESS Maestro 2E PCI audio accelerator (M2E), a high-performance 500-MIPS-equivalent PCI audio processor, uses the high-bandwidth PCI bus and an AC'97 CODEC to deliver advanced PC audio features. These features include HRTF 3-D positional audio, high-quality 64-channel wavetable music synthesis with downloadable wavetable samples, and DVD AC-3 5.1-to-2 speaker virtualization.

The device, shown in Figure 6-1, implements multistream DirectSound and DirectSound3D acceleration and Windows 95 and Windows 98 stream acceleration with digital mixing and sample rate conversion. The M2E maintains full DOS legacy audio compatibility over a standard PCI 2.1 bus. The M2E is designed for high-performance consumer multimedia PC, notebook PC, and add-in card applications.

Based on a dual-engine, 64-channel, pipelined wave processor and a programmable audio signal processor, the M2E provides simultaneous support for multiple audio streams of different types. Its core architecture is designed to handle complex signal processing tasks with a bus-mastering PCI interface and a built-in dedicated DMA engine supporting a DSP core. The support functions ensure efficient transfer of audio data streams to and from system memory buffers, providing a system solution with maximum performance and minimal host CPU loading. The architecture enables implementation of communications over the Internet from multiple sources.

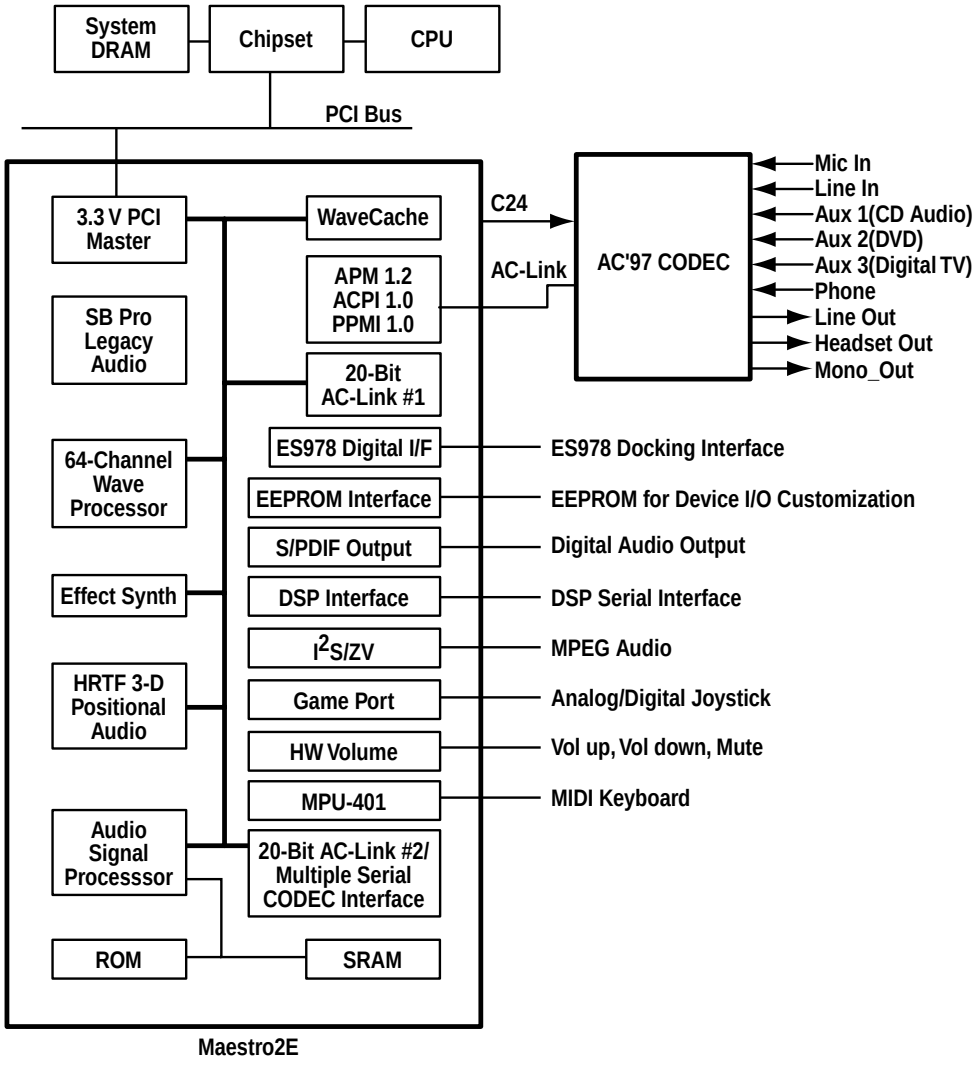

Figure 6-1. *ESS Maestro 2E Block Diagram used in the Armada E500 and Armada V300 Computers*

The M2E has a variety of audio interfaces. It has two internal 20-bit AC'97 CODEC interfaces. The secondary AC'97 CODEC interface is used to handle the Docking station CODEC interface.

The M2E, which operates at 3.3 volts, has several special features for notebook operation, including compliance with the Advanced Power Management (APM) 1.2, Advanced Configuration and Power Interface (ACPI) 1.0, and PCI Power Management Interface (PPMI) 1.0. The M2E has multiple power-saving modes (D0, D1, D2, and D3) for power-efficiency when the audio system is both active and idle. Its high-quality docking solution supports an AC link-based digital docking solution with its secondary 20-bit AC link. The CLKRUN# pin support can be used to stop the PCI interface clock. This helps achieve the lowest power consumption in D3 hot mode.

The device supports full DOS game compatibility for both PC motherboard and add-in card solutions through three hardware implementations: PC/PCI, Distributed DMA (DDMA), and Transparent DMA (TDMA). While PC/ PCI and DDMA are industry-standard protocols for legacy support, ESS's TDMA technology implements DOS game compatibility over the standard PCI 2.1 bus.

Features

High-Performance PCI Audio Acceleration

- 500-MIPS-equivalent dual-engine PCI audio accelerator
- 64-Channel wavetable synthesis
- HRTF 3-D positional audio acceleration
- MultiStream DirectSound and DirectSound3D acceleration
- Hardware acceleration for DirectMusic, ActiveMovie, and DirectInput API
- DVD AC-3 speaker virtualization
- Enhanced effects (reverb, chorus, flange, treble, bass, and 3D stereo expander)
- Advanced platform for interactive 3-D gaming, DVD movie playback, and Internet communications

Legacy DOS Game Support

- Full DOS game compatibility through three hardware implementations: PC/PCI, DDMA, and TDMA
- TDMA needs no sideband signals and achieves full DOS game compatibility in the standard PCI 2.1 bus
- Serial IRQ support

Flexible Audio I/O Interface

- 20-bit AC'97 1.03/2.00 CODEC interface
- I2S Zoomed Video interface
- Two-button hardware master volume control

Digital Ready

- Windows 98 WDM acceleration

Power Management

The M2E is a high-performance device with low power consumption. Besides the low power CMOS technology used to process the M2E, various features are designed into the device to provide benefits from popular power-saving techniques. These features and techniques are discussed in this section.

CLKRUN Protocol

The PCI CLKRUN feature is one of the primary methods of power management on the PCI bus interface of the M2E for the notebook computer.

PCI Power Management Interface (PPMI)

The PCI Power Management Interface (PPMI) specification establishes the infrastructure required to let the operating system control the power of PCI functions. This is done by defining a standard PCI interface and operations to manage the power of PCI functions on the bus. The PCI functions can be assigned one of five power management states that result in varying levels of power savings.

The five power management states of PCI functions are:

- D0–full power
- D1 and D2–intermediate states
- D3 hot–off state; power supply is on
- D3 cold–off state; power supply is off

For the operating system to manage the device power states on the PCI bus, the PCI function supports four power management operations:

- Capabilities reporting
- Power status reporting
- Setting the power state
- System wake-up

The operating system identifies the capabilities of the PCI function by traversing the new capabilities list. The presence of new capabilities is indicated by setting bit [4] in the PCI status register and providing access through a capabilities pointer to a capabilities list.

The capabilities pointer provides access to the first item in the linked list of capabilities. For the Maestro 2E, the capabilities pointer is mapped to an offset, C0h, indicated in the PCI configuration register at 34h. The first byte of each capability register block is required to be a unique ID of the capability. PCI power management has been assigned an ID of 01h. The next byte is a pointer to the next pointer item in the list of capabilities. There are no more items in the list, so the next item pointer is set to zero. The registers following the next item pointer are specific to that function's capability.

The power-management capabilities register (PCI configuration register C2h in the M2E) is a static read-only register that provides information on the capabilities of the functions related to power-management. The power-management control/status register enables control of power-management states and enables and monitors power-management events. The data register is an optional register that displays state-dependent power measurements such as power consumed or heat dissipation.

Disabling Maestro 2E Audio

To disable Maestro 2E audio in both notebook and motherboard implementations:

1. Set PCI 04h[2:0] = 000.

   This disables M2E response to all inputs and outputs and Bus Master cycles.

2. Set PCI 40h[7] = 1.

   This disables M2E response to all legacy audio functions.

WaveCache

The WaveCache dynamically prefetches from the system memory and manages samples for the wave processor (WP). The WaveCache is capable of handling up to 64 separate data streams for the WP. The types of different data streams supported include 16-bit mono, 16-bit stereo, 8-bit mono, 8-bit stereo, and 8-bit differential. The WaveCache also interfaces with the task-oriented signal processor (TOSP) to handle FM synthesis data streams.

Applicable Registers

WaveCache Configurations

The WaveCache has three different configurations:

- WP configuration
- TOSP configuration
- Test configuration

These configurations are set by WaveCache control register bits [0], and [9:7].

The primary configuration, the WP configuration, is where the WaveCache manages samples for the WP. The CPU may write into WaveCache control registers or WaveCache channel buffers using the WaveCache index and data register.

In the TOSP configuration, the WaveCache serves as a general-purpose data buffer for the TOSP. Only the TOSP may access the WaveCache in this configuration.

The Test configuration is for device test purposes, in which only the CPU may read/write the WaveCache. It is enabled by setting bit [0] of the WaveCache control register to 1.

WaveCache Access

The host may access the WaveCache with limitations using the WaveCache Index and Data registers. By setting up the Index register first, the actual read/write to and from the WaveCache registers occur when the indexed data register is read or written. The host may write to the WaveCache in either WP configuration or Test configuration modes, but may only read from the WaveCache when in Test configuration mode.

Wavetable Base Address (R/W)

The twelve Wavetable base address registers allow up to four disjoint table addresses to be specified. The purpose of these registers is to allow the WP channels to deal with only logical addresses.

The M2E supports wavetable sizes from 1 MB to 8 MB in system memory. This wavetable is divided into four equal sizes and these wavetable quarters can reside in physically disjoint locations mapped by the twelve base address registers. Depending on the different wavetable sizes, different top channel address bits (2 bits) are used to select the corresponding base address register and thus the quarter wavetable. Physical address is calculated by adding the base address and the WP address together.

Audio Docking Solution

When docked, the audio output only generates from the docking base. The notebook internal speakers cannot be functional and the audio amplifier is disabled by way of the AUDIO_DOCKED and HP_ON signals. Selecting between input channels from the notebook and the docking station is done by the user through ESS Windows application software. This allows each individual input source to be enabled or disabled. These include microphone inputs and CD-ROM audio.

The audio docking interface consists of an AC97 interface.

Mono Full Duplex Mode

The Maestro 2E allows host-based software applications to use full-duplex mode through two 8-bit DMA channels. However, both record and play must be monophonic, and record and playback are restricted to the same sample rate.

Other Register Bits

The read-only position register is located at Maestro 2E_Base+D2h and Maestro 2E_Base+D4h. Bits [4:0] of Maestro 2E_Base+D2h is the byte number for the current position. When set to 1, bit [0] of Maestro 2E_Base+D2h is the software reset for interface logic. When set to 0, operation is normal (default).

ES1921 Audio CODEC

Description

The ES1921 CODEC is a fully compliant AC'97 CODEC and mixer for an AC'97 digital audio controller embodied in a single, mixed signal chip. Used with the ESS Maestro PCI digital audio controller, the ES1921 implements a high-performance accelerated PCI audio AC'97 solution. The ES1921 is equipped with a stereo 18-bit DAC, a stereo 18-bit ADC, seven inputs (four stereo and three mono), three outputs (two stereo and one mono), and a time division multiplexed (TDM) serial AC-Link to a Maestro Digital Controller.

The ES1921 audio CODEC can record and play back voice, sound, and music at 48 KHz sample rate. The playback mixer has five stereo inputs (Line, CD, Video, Aux, and PCM digital audio) and three mono inputs (Mic, Phone, and PC beep). The record multiplexer has five stereo inputs (Line, CD, Video, Aux, and Mixer) and three mono inputs (Mic, Phone, and Mono mix). The mixer has three outputs (Line, True Line Level, and Mono). Line out can be used for stereo output to multimedia speakers, while Mono out can be used to output to a telephony subsystem or a down-line phone. True Line Level out can be used for DVD applications at a 96 KHz sample rate or any other consumer equipment–compatible application.

Applications

- Multimedia PCs
- 3-D PC Games
- Music Synthesis
- Business Audio
- DVD-ROM/Consumer Video Audio Playback
- Audio Conferencing
- Voice Recognition

Features

- Single, high-performance, mixed-signal, 18-bit stereo VLSI chip
- Meets or exceeds Audio CODEC ’97 revision. 2.1 and Audio CODEC ’97 revision 1.3 analog performance specifications
- Supports 2-CODEC architecture for notebook and docking station configuration with one ES1921 in each
- Supports direct Digital Audio mode data out and PCM data in implementing full digital-ready audio support
- AC-Link digital serial interface (TDM format) to a Maestro Digital Controller

Record and Playback Features

- Full-duplex stereo operation for simultaneous record and playback
- 18-bit stereo ADC and DAC
- 18 KHz playback and record sample rate
- True Line Level Out handles 96 KHz sample rates

Inputs/Outputs

- Stereo inputs for line-in and CD
- Two selectable mono inputs for microphone sharing of a single mixer input and one mono input for phone
- PC speaker input
- Stereo output for line-out

Power

- Advanced Configuration and Power Interface (ACPI) support
- 5.0 volt analog and 3.3 volt digital power supply

Compatibility

- Meets Microsoft PC97 and PC98 1.0 specifications for Baseline and Advanced Audio with FAQ updates
- Meets Intel’s Audio CODEC ’97 1.03 and 2.1 specifications

Functional Description

This section shows the overall structure of the ES1921 and discusses its major functional subunits. The major subunits of the ES1921 are shown in Figure 6-2 and described briefly in the following paragraphs.

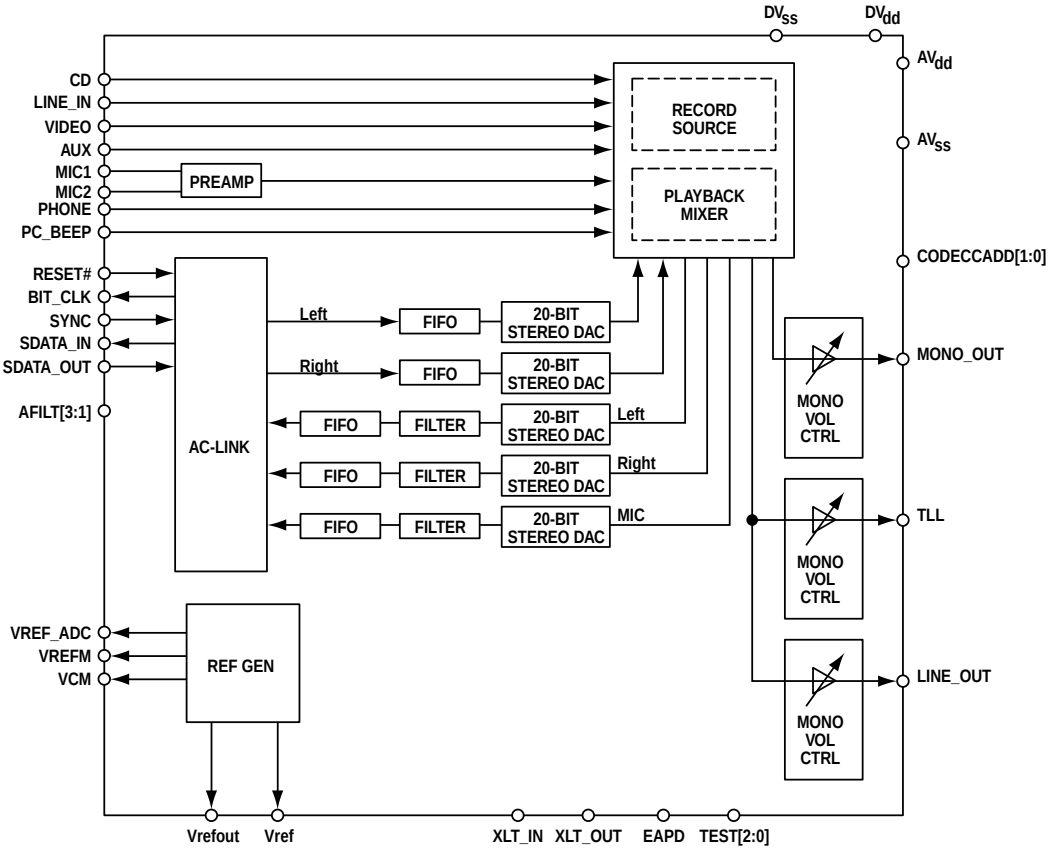

Figure 6-2. *ESS1921 Block Diagram*

Digital Subsystems

- **AC-Link–**A four-line serial link between the ES1921 and a Maestro Digital Controller. The fifth line, RESET#, is linked directly to the host. This link is the control interface for the ES1921. It also carries audio data between the ES1921 and its Maestro Digital Controller.

Analog Subsystems

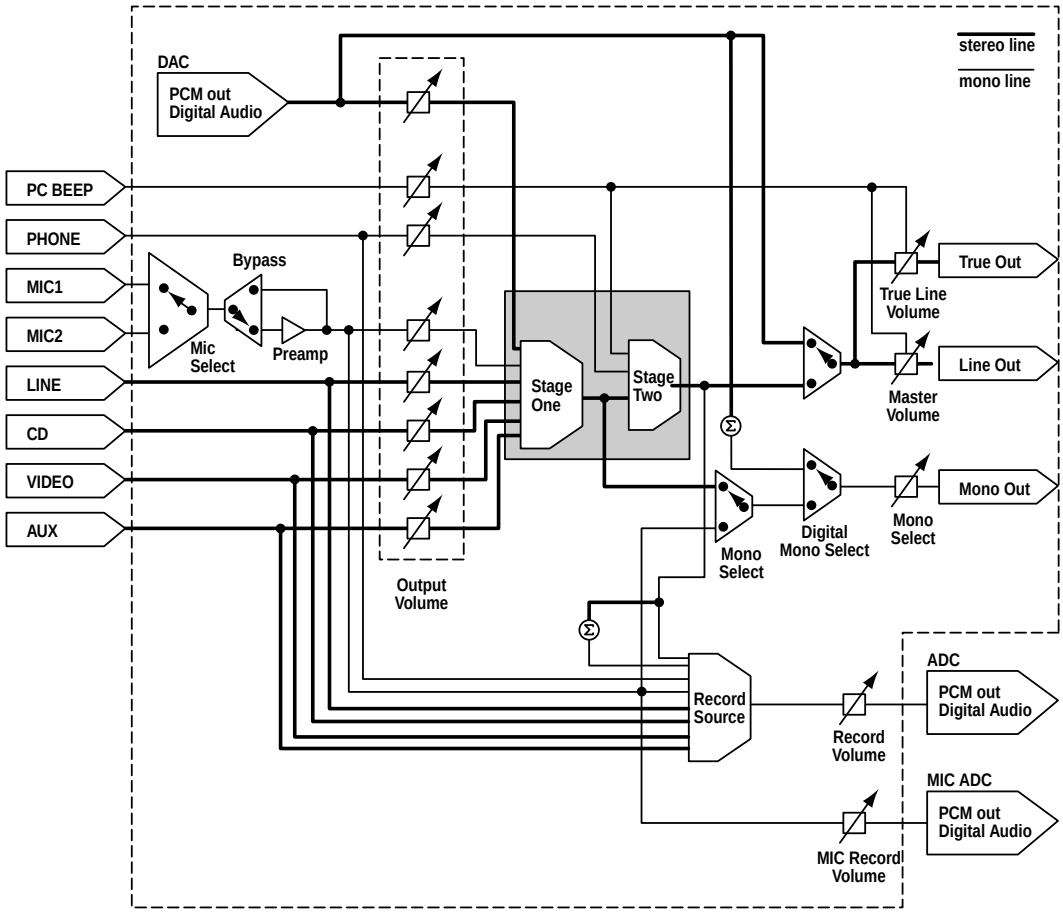

Figure 6-3. ESS1921 Mixer Block Diagram

- **Playback Mixer**–eight input stereo mixer, shown in Figure 6-3. Each of these inputs except PC_BEEP has 5-bit volume control:
  - PCM out (digital audio from the Maestro Digital Controller)
  - Line in
  - CD audio In
  - Video audio in
  - Auxiliary in
- Each of these inputs has volume control bits as shown:
  - PC beep throughput (4 bits)
  - Phone in (6 bits)
  - Mic1 or Mic2 mono In (6 bits)
- **18-bit stereo DAC–**for audio playback of digital audio from the Maestro Digital Controller. (DAC can operate with 96 KHz sample rate data; sample stream is interpolated. Output is antialiased and band-limited to 20 KHz).

- **18-bit stereo ADC–**for audio record. Audio is returned to the host through the AC-Link and the Maestro Digital Controller.
- **18-bit mono MIC ADC–**for speakerphone applications. Data can be used for echo cancellation. Audio is returned to the host through the AC-Link and the Maestro Digital Controller.
- **Record source and input volume control–**input source and volume control for recording. The Mic source can be mixed post-input volume with its own independent input volume control. The recording source can be selected from one of eight choices:
  - Line in
  - CD audio in
  - Auxiliary in
  - Video audio in
  - Stereo mix
  - Mono mix
  - Mic in
  - Phone
- **Output volume and mute–**The output master volume supports 6 bits per channel plus mute. There are separate volume controls for mono out and stereo out.
- **Reference generator–**analog reference voltage generator.
- **Filter–**switched capacitor low-pass filter. For DAC, simple anti-alias filter at ADC input.
- **Pre-amp**–20-dB microphone preamplifier with bypass.

Double-Rate Audio Playback

To support 96 KHz DVD “pure audio” applications, the ES1921 provides for double-rate audio playback. Normally, the ES1921 plays back 48 KHz data received from outgoing slots 3 and 4. To play back 96 KHz data, the ES1921 uses twice the number of slots, adding slots 10 and 11 to slots 3 and 4 to carry the left and right PCM audio data.

Double-rate audio mode is enabled by setting the DRA enable bit high (extended audio control and status register 2Ah bit 1).

Digital Audio Mode

Digital audio mode, shown in Figure 6-4, is a means of providing digital-ready audio support. The final rendered audio can be routed to multiple locations. In the case of the ES1921, the output of the playback mixer is routed to the ADC and back to the digital controller, where the digital audio can be distributed. This audio data comes back to the ES1921 through the AC-link and is passed through the DAC, through the DAC analog volume control, to the Line_Out or True Line_Out volume controls, and then the outputs. This is achieved by switching the digital audio mode bit. Set bit [6] of register 5Ch high to enable digital audio mode.

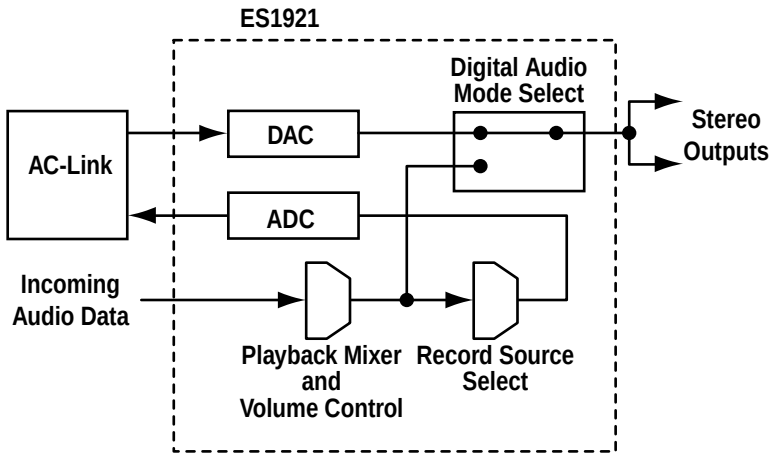

***Figure 6-4**. ESS1921 Digital Audio Mode Select Block Diagram*

Digital Interface

The ES1921 uses a digital serial interface to link with a Maestro Digital Controller. This link (the AC-Link) uses a bidirectional, fixed-rate, serial PCM digital stream. It carries multiple input and output streams, as well as the control register information. To achieve these, the AC-Link uses a time division multiplexed (TDM). Reference to outgoing and incoming data streams (or time slots) are made from the point of view of the Maestro Digital Controller. Therefore, an outgoing stream is sent from the Digital Controller to the ES1921. An incoming stream is sent from the ES1921 to the Maestro Digital Controller.

AC-Link Digital Serial Interface Protocol

Each audio frame of the digital serial stream is divided into 12 incoming and 12 outgoing data streams. The ES1921 implements 20-bit resolution within each data stream.

The following data streams or slots are used by the ES1921:

- **PCM playback** **Two transmit slots**

  Two-channel composite PCM transmit stream which can be programmed to use two of eight slots

- **PCM double-rate playback** **Two transmit slots**

  Two-channel composite PCM transmit stream which is used for double-rate audio

- **PCM record** **Two receive slots**

  Two-channel composite PCM receive stream

- **Control** **Two transmit slots**

  Control register write and data ports

- **Status** **Two receive slots**

  Control register read and data ports

- **Dedicated MIC input** **One receive slot**

  One-channel composite PCM receive stream

Transmit slots are sent from the Maestro Digital Controller to the ES1921. Receive slots are received by the Maestro Digital Controller from the ES1921.

Synchronization of all AC-Link data transactions is signaled by the Maestro Digital Controller. The ES1921 drives the serial bit clock onto the AC-Link, which the Maestro Digital Controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support twelve 20-bit outgoing and incoming time slots. AC-Link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-Link data, the ES1921 for outgoing data and Maestro Digital Controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

Tag Phase

The first 16 cycles of each audio frame is called the tag phase. During the tag phase SYNC is high. The AC-Link protocol provides for this special 16-bit time slot (Slot 0), in addition to the other twelve 20-bit slots. Each bit in slot 0 represents a valid tag for its corresponding time slot within the current audio frame. A “1” in the assigned bit position of Slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream and contains valid data. If a slot is “tagged” invalid, the data is ignored.

The remainder of the audio frame is called the data phase. During this phase, SYNC is low.

AC-Link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the ES1921's DAC inputs and control registers. As was previously discussed, each audio output frame supports up to 12 outgoing 20-bit data time slots. In addition, Slot 0 is a special reserved time slot containing 16 bits. This time slot is used to tag which data time slots carry valid data.

Within Slot 0, the first bit (SDATA_OUT Slot 0, bit 15) flags the entire audio frame as valid or invalid.

A new audio output frame begins on the rising edge of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the falling edge of BIT_CLK immediately following, the ES1921 samples the assertion of SYNC. This falling edge marks the time when both sides of the AC-Link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the Maestro Digital Controller transitions SDATA_OUT into the first bit position of Slot 0 (Valid Frame bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK, and is subsequently sampled by the ES1921 on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

If this bit, the Valid Frame bit, is a 1, then the current audio frame contains at least one time slot of valid data. The next 12 bit positions sampled by the ES1921 indicate which of the corresponding 12 time slots contain valid data. This allows for data streams of differing sample rates to be transmitted across the AC-Link at its fixed 48 KHz audio frame rate. If the Valid Frame bit is a 0, the ES1921 ignores all the data in the rest of the frame.

The SDATA_OUT composite stream is MSB justified (MSB first) with zeroes stuffed in the bit positions of all non-valid slots by the Maestro Digital Controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the Maestro Digital Controller always stuffs all trailing non-valid bit positions of the 20-bit slot with zeroes. As an example, consider an 8-bit sample stream that is being played out to one of the ES1921 DACs. The first 8-bit positions are presented to the DAC (MSB justified). The next 12 bit positions are stuffed with zeroes by the Maestro Digital Controller. This ensures that regardless of the resolution of the implemented DAC (16-, 18-, or 20-bit), no DC biasing is introduced by the least significant bits.

When mono audio sample streams are output from the Maestro Digital Controller, both the left and right sample stream time slots are filled with the same data.

Power Management

The ES1921 is capable of operating at reduced power when no activity is required. The state of power-down is controlled by the power-down control/status register (26h). There are seven separate power states: PR0 through PR6.

Figure 6-5 illustrates an example procedure for powering down the ES1921. From normal operation, sequential writes to the power-down control/status register 26h are performed to power down the ES1921 subsection by subsection. After everything has been powered down, a final write (of PR4) shuts down the AC-Link. The ES1921 remains in sleep mode with all its registers holding their static values.

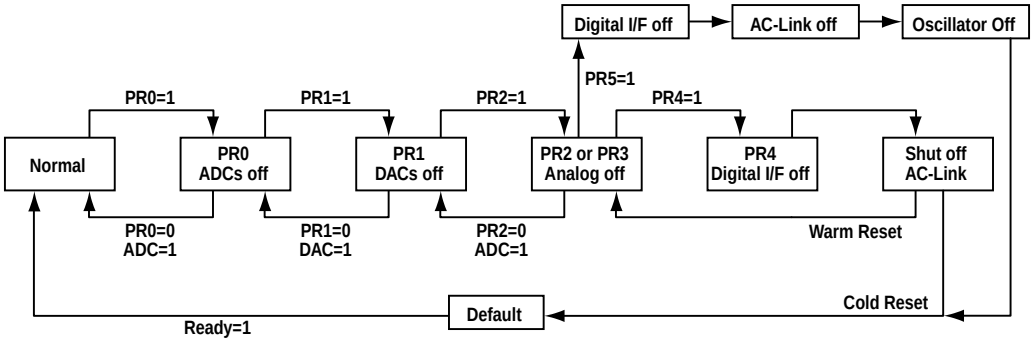

Figure 6-5. *Example of Power-Down/Power-Up Flow*

A warm reset or a cold reset returns the ES1921 to a wakened state. To wake up the ES1921, the Maestro Digital Controller sends a pulse on the SYNC line issuing a warm reset. This restarts the AC-Link (resetting PR4 to zero). A cold reset also wakes up the ES1921. However, a cold reset causes a loss of context, as a cold reset returns the ES1921 registers to their default states. When a subsection is powered back on, the power-down control/status register 26h should be read to verify that the subsection is ready (stable) before attempting any operation that requires that subsection.

Figure 6-6 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through the ES1921 to the speakers but have most of the system in low-power mode. The procedure for invoking this state follows the previous example except that the analog mixer is never shut down. The exception is in PR5: the analog is shut down when a cold reset occurs.

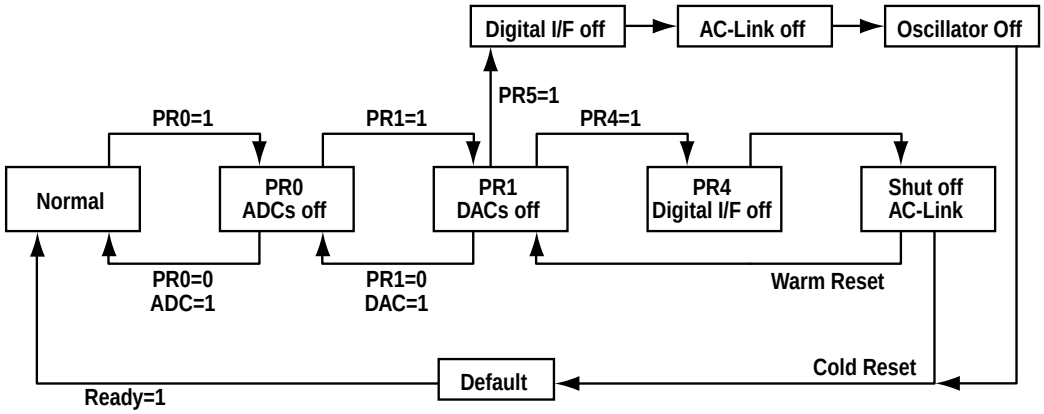

***Figure 6-6**. ESS1921 Mixer Static Volume Settings*

When PR3 is set to 1, ADC, DAC, Mixer, and Vref are powered down no matter what the state of PR[3:0]. When PR3 is reset to 0, ADC, DAC, Mixer, and Vref are returned to their previous states as determined by the state of PR[3:0]. When these subsections are powered down (ADC, DAC, Mixer, and Vref), the ES1921 flags the appropriate slots as invalid in Slot 0 of the audio input frame.

Audio Linear Amplifier LM4873

The LM4873 is a dual bridge-connected audio power amplifier which, when connected to a +5V supply, will deliver 2.1W to a 4 Ohm load with less than 1.0% THD+N. In addition, the headphone input pin allows the amplifiers to operate in single-ended mode to drive stereo headphones. A Mux Control pin toggles between the two stereo sets of amplifier inputs, allowing for two select-able amplifier closed-loop responses. To simplify audio system design, the LM4873 combines dual bridge speaker amplifiers and stereo headphone amplifiers in one chip. The LM4873 features an externally controlled, low-power consumption shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection. It also utilizes circuitry to reduce ‘clicks and pops’ during device turn-on.

chapter 7

VIDEO/GRAPHICS SUBSYSTEM

This chapter describes the general video/graphics subsystem architecture found in the Armada E500 and Armada V300 computers. For detailed information regarding components used in this subsystem, refer to the particular component's data sheet. The video/graphics subsystem provides desktop-level performance through advanced multimedia acceleration and integrated 64-bit 2D and 3D graphics acceleration with XGA flat panel and/or CRT displays. The graphics controller used in the Armada E500 and Armada V300 is the ATI Technologies RAGE Mobility-P, with 8 MB and 4 MB of video memory, respectively.

General Features

- High integration provides a low-cost, low-power, one component graphics subsystem ideal for a full range of notebook designs
- Comprehensive AGP support, including 1X and 2X mode, sideband addressing, and AGP texturing
- PCI version 2.1 with full bus mastering and scatter/gather support
- Fully PC 98/PC 99 compliant
- Bi-Endian support for compliance on a variety of processor platforms
- Fast response to host commands
- Triple 8-bit palette DAC with gamma correction for true WYSIWYG color and pixel rates up to 230 MHz
- ACPI/On Now architecture compliance
- DDC1 and DDC2B+ supporting EDID 2.0 for plug and play monitors
- Integrated 112-MHz dual-channel LVDS transmitters
- Integrated motion compensation and IDCT circuitry
- Integrated hardware diagnostic tests performed automatically upon initialization

Video Interface

The RAGE Mobility-P integrates the flat panel/VGA controller, 2D/3D graphics acceleration hardware, motion compensation of MPEG-2 data, memory controller with a 64-bit data path, RAMDAC, clock synthesizer, Zoomed Video interface, and LVDS control interface into a single package. The Mobility-P interfaces to the system through the AGP bus for maximum performance, and supports Zoomed Video.

The controller provides all current compatible modes, including VGA, SVGA, and XGA modes. It supports the internal single-interface or dual-interface LCD panels as well as an external CRT and TV monitor. Simultaneous display is supported on the LCD and CRT, CRT and TV, or LCD and TV.

Figure 7-1 provides a block diagram for the controller.

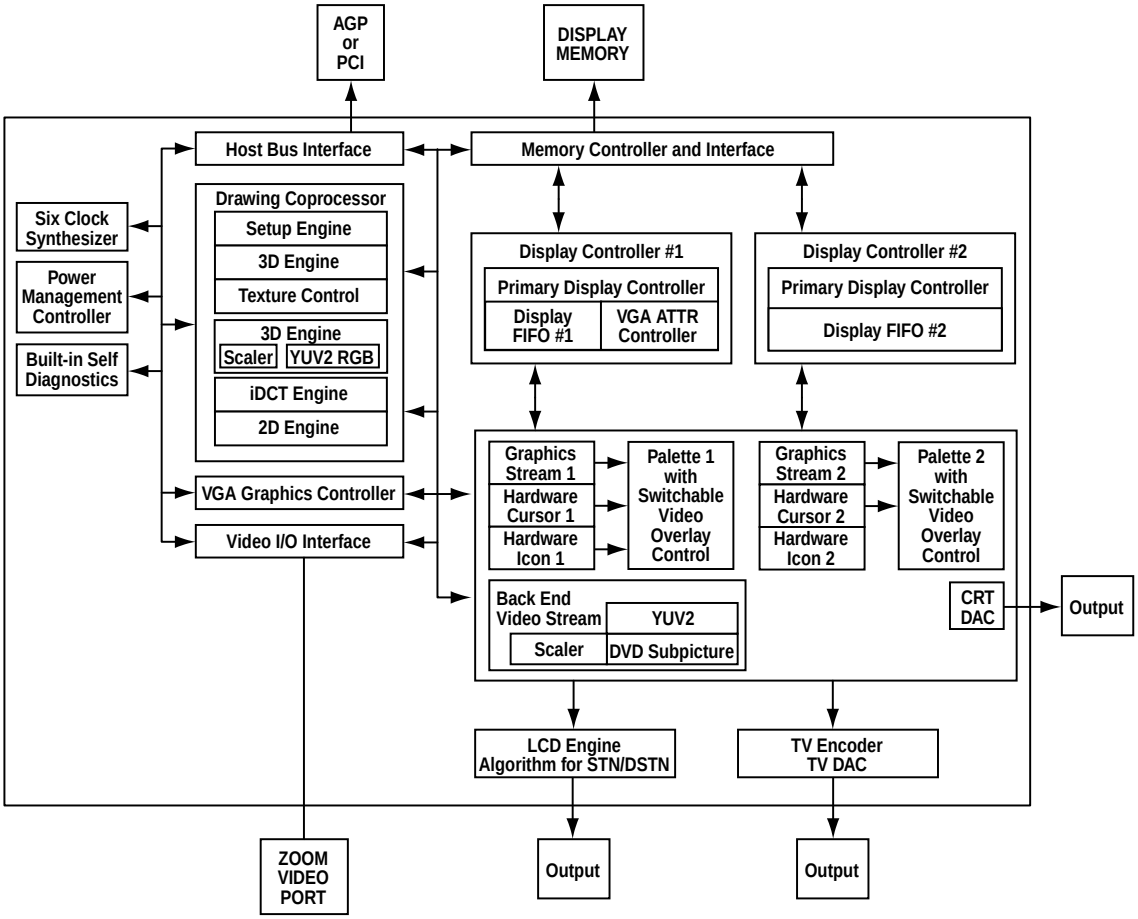

Figure 7-1. *RAGE Mobility-P Graphics Controller used in the Armada E500 and Armada V300*

The video interface is hardware and register compatible with the VGA standard. This device uses a 2.5-volt video controller core voltage and provides external high resolution video and a variety of LCD panel support. The RAGE Mobility-P supports full SimulScan operation, where the two displays can not only have different resolutions, pixel depths, and refresh rates, but–with proper OS support–different video data.

This device provides hardware and register compatible VGA video drivers to support 640 × 480, 800 × 600, and 1024 × 768 panels, with up to 16M colors on 24-bit active matrix panels, as well as up to 1600 × 1200 pixels and 100-Hz refresh support (not simultaneously) for external monitors. The controller also utilizes the 32-bit AGP bus interface and the 64-bit memory interface for significantly improved video performance.

The Mobility-P is capable of overlaying MPEG-2 video on top of the display data, creating a scalable MPEG window of full motion video, while continuing to produce standard PC video output. It can also convert either or both of these data streams to NTSC or PAL output format and channel this data to a standard TV interface.

Bus Interface

The RAGE Mobility-P provides the following:

- Direct 32-bit AGP bus interface at 2X clocking with all sideband signals
- 64-bit interface to video memory

Options such as internal decoding of all memory and I/O addresses, bus width translations, and generation of necessary control signals are handled in a fashion transparent to the CPU.

Power Management

Power management for the video controller includes disabling the 3D engine, motion compensation circuitry, and CRT interface when not needed; eliminating power to the LCD interface; and powering down the backlight. In the Suspend-to-DRAM state, the video controller and video memory remain powered, but in a stand-by state. For details of the video power management, refer to Appendix B.

Video Controller Clock Generation

The integrated clock synthesizer in the RAGE Mobility-P generates a variety of programmable memory clock and dot clock frequencies, such that a wide variety of display resolutions and vertical refresh rates are supported.

Flat Panel Support

The RAGE Mobility-P can provide support for different flat panels. The Armada E500 supports a 14.1- or 15.1-inch XGA, TFT (1024 × 768) display, using the low voltage differential signaling (LVDS) interface. The Armada V300 supports a 12.1-inch SVGA, STN (800 x 600) CMOS display or a 14.1-inch XGA, TFT (800 x 600) LVDS display. Both computers also support a 12.1-inch SVGA, TFT (800 x 600) LVDS display.

CRT

The RAGE Mobility-P supports high-resolution variable frequency analog monitors in interlaced and non-interlaced modes of operation. Other than color depth, the modes supported by the Mobility-P apply to both the LCD and the CRT. The exception to this is the 1280 × 1024 and 1600 × 1200 modes, which are supported for the CRT only.

The external video interface is capable of supporting all VGA-compatible monitors with a horizontal scan frequency of 31.49 KHz and a vertical refresh rate of 60 to 100 Hertz. The external video signals are analog RGB at 0 to +0.714 volts full scale, with zero volts representing black. Output impedance is 75 ohms. The color DAC is powered by Vcc at 5 volts.

When an external monitor is attached, the video circuit detects the type of monitor (monochrome or color) present using the analog voltage comparator method, and automatically configures itself for the proper operating mode. This same method is used to determine if a monitor is present during a resume operation.

The DDC (display data channel) 2B specification is also supported. This uses an I^2C interface to determine a CRT monitor's capabilities.

2D Acceleration

The RAGE Mobility-P has built-in 2D video acceleration including the following:

- Hardware acceleration of Bit-BLT, line draw, polygon/rectangle fill, bit masking, monochrome expansion, panning/scrolling, and scissoring
- Hardware cursor support (up to 64 × 64 pixels × 2 colors)
- Game acceleration with support for the Microsoft's DirectDraw–double buffering, virtual sprites, masked BLT, transparent BLT, and context chaining
- Acceleration in 8, 16, 24, 32 bit per pixel modes

3D Acceleration

The controller has built-in 3D video acceleration, including the following:

- Integrated 1.2 million triangle per second setup engine
- 4 KB on-chip texture cache for 3D primitives
- Complete 3D primitive support–points, lines, triangles, lists, strips, quadrilaterals, and BLTs with Z-compare
- Full screen or window double buffering
- Hidden surface removal using 16-bit Z-buffering
- Edge anti-aliasing
- Subpixel and subtexel accuracy
- Gouraud and specular-shaded polygons
- Perspective-corrected mip-mapped texturing with chroma-key support
- Support for single pass bi- and tri-linear texture filtering
- Full support of Direct3D texture lighting

TV Out

The RAGE Mobility-P supports standard 50-Hz and 60-Hz TV monitors in interlaced operation. All CRT color depths are supported.

A television monitor has unlimited color depth so it can support whatever colors the video controller supports; the Mobility-P supports up to 32-bit colors.

The external TV interface supports the formats listed in Table 7-1.

Table 7-1
World TV Standards Supported

NTSC-M	PAL-I	PAL B, G, or H		PAL-N	PAL-M	PAL-D
Antigua	Angola	Albania	Malta	Argentina	Brazil	China
Aruba	Botswana	Algeria	Monaco	Paraguay		N. Korea
Bahamas	Gambia	Australia	Mozambique	Uruguay		Romania
Barbados	Guinea-Bissau	Austria	Nepal			
Belize	Hong Kong	Bahrain	Netherlands			
Bermuda	Ireland	Bangladesh	New Zealand			
Bolivia	Lesotho	Belgium	Nigeria			
Burma	Malawi	Bosnia	Norway			
Canada	Namibia	Cambodia	Oman			
Chile	Nigeria	Cameroon	Pakistan			
Colombia	South Africa	Croatia	Papua New Guinea			
Costa Rica	Tanzania	Cyprus	Portugal			
Cuba	U.K.	Denmark	Qatar			
Curacao	Zanzibar	Egypt	Romania			
Dominican Republic		Ethiopia	Saudi Arabia			
Ecuador		Equatorial Guinea	Seychelles			
El Salvador		Finland	Sierra Leone			
Guam		Germany	Singapore			
Guatemala		Ghana	Slovenia			
Honduras		Gibraltar	Somali			
Jamaica		Greenland	Spain			
Japan		Iceland	Sri Lanka			
S. Korea		India	Sudan			
Mexico		Indonesia	Swaziland			
Montserrat		Israel	Sweden			
Myanmar		Italy	Switzerland			
Nicaragua		Jordan	Syria			
Panama		Kenya	Thailand			
Peru		Kuwait	Tunisia			
Philippines		Liberia	Turkey			
Puerto Rico		Libya	United Arab Emirates			
Samoa		Luxembourg	Uganda			
Suriname		Malaysia	Yemen			
Taiwan		Maldives	Zambia			
Trinidad			Zimbabwe			
Tobago						
USA						
Venezuela						
Virgin Islands						

NOTE: The differences between all PAL variants except PAL-M are minor, in the context of PC video. These variants are all grouped as one type (called 'PAL') in the ATI video BIOS.

Simultaneous Scan Mode

The RAGE Mobility-P provides simultaneous display operation with Multisync variable frequency CRT, PS/2 fixed frequency CRT, or TV monitors and SS or DS LCDs. Resolutions, refresh rates and display data can be independent. Scanning is supported in high-resolution modes. A 640 × 480 LCD panel can be used in simultaneous mode with a CRT at 1024 × 768 (or 800 × 600) using scanning. The LCD panel displays only a 640 × 480 portion of the 1024 × 768 (or 800 × 600) display. This portion may be scrolled to different areas of the higher resolution display with either a keyboard or pointing device. This allows the user to disconnect the CRT and still be able to read the flat panel when in high-resolution modes.

The system has the capability of driving both the LCD display and the external CRT display simultaneously as well as switching between them. The LCD/CRT switching is handled by the RAGE Mobility-P and is controlled via **Fn-F4** key.

Video Mode Support

The following single and double video modes are supported by the RAGE Mobility-P. Some modes may not be available in all operating systems.

- Single Display Modes
- Dual Display Modes
- DVD (MPEG-2) Display Modes
- TV Display Modes

Single Display Modes

The RAGE Mobility-P supports the video modes illustrated in Table 7-2 when using a single display (LCD or CRT):

Table 7-2
Single CRT Supported Modes (TFT or DSTN or CRT)

			Minimum amount of Memory Required			
dsp wid	**dsp hgt**	**ref (Hz)**	**8bpp**	**16bpp**	**24bpp**	**32bpp**
640	480	60	2 MB	2 MB	2 MB	2 MB
640	480	72	2 MB	2 MB	2 MB	2 MB
640	480	75	2 MB	2 MB	2 MB	2 MB
640	480	90	2 MB	2 MB	2 MB	2 MB
640	480	100	2 MB	2 MB	2 MB	2 MB
800	600	60	2 MB	2 MB	2 MB	4 MB
800	600	70	2 MB	2 MB	2 MB	4 MB
800	600	75	2 MB	2 MB	2 MB	4 MB
800	600	90	2 MB	2 MB	2 MB	4 MB
800	600	100	2 MB	2 MB	2 MB	4 MB
1024	768	60	2 MB	2 MB	4 MB	4 MB
1024	768	72	2 MB	2 MB	4 MB	4 MB
1024	768	75	2 MB	2 MB	4 MB	4 MB
1024	768	90	2 MB	2 MB	4 MB	4 MB
1024	768	100	2 MB	2 MB	4 MB	4 MB
1280	1024	43	2 MB	4 MB	4 MB	8 MB
1280	1024	60	2 MB	4 MB	4 MB	8 MB
1280	1024	70	2 MB	4 MB	4 MB	8 MB
1280	1024	72	2 MB	4 MB	4 MB	8 MB
1600	1200	60	4 MB	4 MB	8 MB	8 MB
1600	1200	66	4 MB	4 MB	8 MB	8 MB
1600	1200	76	4 MB	4 MB	8 MB	8 MB
1600	1200	85	4 MB	4 MB	8 MB	8 MB

NOTE: Video modes supported by the RAGE Mobility-P but requiring greater than 4 MB of video memory are not shown.

NOTE: Video resolutions greater than 1024 × 768 are not supported by the LCD display. Refresh rates other than 60 Hz are not used by the LCD display.

Dual Display Modes

The RAGE Mobility-P supports the following video modes when using two displays simultaneously (LCD + CRT), each displaying a different image.

Table 7-3
Dual Display Modes

LCD Resolution	CRT Resolution
1024 × 768 8 bpp	640 × 480 up to 32 bpp 800 × 600 up to 32 bpp 1024 × 768 up to 32 bpp 1280 × 1024 up to 24 bpp 1600 × 1280 up to 8 bpp
1024 × 768 16 bpp	640 × 480 up to 32 bpp 800 × 600 up to 32 bpp 1024 × 768 up to 32 bpp 1280 × 1024 up to 16 bpp 1600 × 1280 up to 8 bpp
1024 × 768 24 bpp	640 × 480 up to 32 bpp 800 × 600 up to 32 bpp 1024 × 768 up to 32 bpp 1280 × 1024 up to 16 bpp 1600 × 1280 not supported
1024 × 768 32 bpp	640 × 480 up to 32 bpp 800 × 600 up to 32 bpp 1024 × 768 up to 32 bpp 1280 × 1024 up to 8 bpp 1600 × 1280 not supported

DVD (MPEG-2) Display Modes

The RAGE Mobility-P supports the following video modes when playing back MPEG-2 data in a scalable window, using the built-in motion compensation logic (LCD or CRT):

Table 7-4
DVD (MPEG-2) Display Modes with Software MPEG Decoding

			Minimum Required Memory with DVD NTSC Format				Minimum Required Memory with DVD PAL Format			
dsp iwid	**dsp hgt**	**ref(Hz)**	**8bpp**	**16bpp**	**24bpp**	**32bpp**	**8bpp**	**16bpp**	**24bpp**	**32bpp**
640	480	60	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640	480	72	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640	480	75	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640	480	90	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
640	480	100	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB
800	600	60	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	
800	600	70	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	
800	600	75	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	
800	600	90	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	
800	600	100	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	4 MB	
1024	768	60	4 MB	4 MB			4 MB	4 MB		
1024	768	72	4 MB	4 MB			4 MB	4 MB		
1024	768	75	4 MB	4 MB			4 MB	4 MB		
1024	768	90	4 MB	4 MB			4 MB	4 MB		
1024	768	100	4 MB	4 MB			4 MB	4 MB		
1280	1024	43	4 MB				4 MB			
1280	1024	60	4 MB				4 MB			
1280	1024	70	4 MB				4 MB			
1280	1024	74	4 MB				4 MB			

NOTE: Video modes supported by the RAGE Mobility-P but requiring greater than 4 MB video memory are not shown. Video resolutions greater than 1400 × 1050 are not supported by the LCD display. Refresh rates other than 60 Hz are not used by theLCD display.

TV Display Modes

The RAGE Mobility-P supports the following video modes when using an NTSC or PAL television or monitor:

Table 7-5
TV Display Modes (any Color Depth Without Panning)

Mode	NTSC (60 Hz)	PAL (50 Hz)
320 × 350	yes	yes
320 × 400	yes	yes
320 × 480	yes	yes
360 × 400	yes	yes
400 × 600	yes	yes
512 × 384	yes	yes
640 × 350	yes	yes
640 × 400	yes	yes
640 × 480	yes	yes
720 × 350	yes	yes
720 × 400	yes	yes
720 × 480	yes	yes
704 × 480	yes	yes
800 × 600	yes	yes
512 × 768	yes	yes
640 × 768	yes	yes
848 × 480	yes	yes
1024 × 768	yes	yes
1024 × 600	as 1024 × 600	as 1024 × 600

Video Memory

The video system uses 8 MB (Armada E500) or 4 MB (Armada V300) of 125-MHz SDRAM as graphics memory. The RAGE Mobility-P uses a 64-bit data path to display memory. Display memory control signals are derived from the integrated clock synthesizer's memory clock. The RAGE Mobility-P serves as a DRAM controller for the video display memory. It handles DRAM refresh, fetches data from display memory for display refresh, interfaces the CPU and 82443BX to display memory, and supplies all necessary DRAM control signals. For the Armada E500 and Armada V300, self-refreshing DRAMs are used, eliminating the need to provide refresh-clocking signals during suspend-to-RAM.

Zoomed Video

Zoomed Video is a way to get real-time video into the video controller without using up bus bandwidth or CPU cycles. It utilizes a 16-bit video port on a video controller that accepts YUV data, the same style port that is used for the VESA advanced feature connector in some desktops.

Motion Video Acceleration

- Hardware DVD decode through integrated motion compensation and iDCT circuitry for full frame rate DVD playback
- Smooth video scaling and enhanced YUV to RGB color space conversion for full-screen/full-speed video playback
- Front and back end scalers support multistream video for video conferencing and other applications
- Enhanced line buffer allows vertical filtering of native MPEG-2 size (720 × 480) images
- Switchable video overlay with DVD subpicture in either primary or secondary CRTC
- Bidirectional bus mastering engine with planar YUV to packed format converter for MPEG-2
- Hardware mirroring for flipping video images
- Direct YUV path to TV encoder

chapter 8

KEYBOARD/POINTING DEVICE SUBSYSTEM

The internal keyboard for the Armada E500 and Armada V300 computers consists of a keyboard matrix with a keyboard controller integrated into the MSIO Super I/O Controller, a TouchPad, or stickpoint pointing device (depending on computer model) and select buttons. The computers and optional convenience base have a connector for an external full-sized keyboard and external mouse.

Internal Keyboard

The keyboard used with the Armada E500 and Armada V300 computers is designed to allow for both TouchPad and EasyPoint pointing devices. Electrically the keyboard emulates a standard 101-key keyboard.

TouchPad Interface

The TouchPad is the Synaptics TouchPad module. It is an input-pointing device that detects the position of a finger over a touch-sensitive area. To move the cursor, the user lightly slides a finger over the smooth sensor area. To select a screen icon, the user gently taps the surface of the TouchPad.

The TouchPad is a capacitive sensor. The user's finger is detected by measuring its effect on an array of capacitive lines integrated into the PC board. The pad senses both the finger's position and its contact area (X, Y, Z). The area of contact is a measure of applied pressure by the user.

One side of the module PC board is the sensor surface, which is a sensitive area protected by a layer of smooth durable Mylar. The other side of the PC board is used for electrical components.

The TouchPad communicates with the system through a standard PS/2 interface and is fully compatible with the standard Microsoft mouse driver. The module connector includes the PS/2 signal pins, power supply pins, and two connections for external mouse buttons.

The TouchPad includes a special edge-sensitive feature that allows the user to extend the drag operation when a finger reaches the edge of the sensor pad. The cursor continues to coast in the indicated direction when the finger is held against the edge.

The system includes driver and application software that allows the user to configure the pad to:

- Adjust touch sensitivity from light to heavy
- Enable or disable tap gestures for left-button or right-button drag
- Enable or disable simulation of a scrolling wheel
- Enable or disable drag lock
- Enable or disable edge motion
- Select two- or three-button mode
- Select 40 or 80 sample per second mode

For further information, refer to the *Synaptics TouchPad Interfacing Guide*.

Touchpad Connections

The TouchPad interface consists of a PS/2 port and left and right button inputs. The left and right buttons generate inputs to the TouchPad. The TouchPad movement and button presses are all transmitted over the PS/2 interface to the MSIO.

EasyPoint IV (Pointing Stick)

The EasyPoint IV assembly consists of a CTS C106-4 mechanical stick integrated into the keyboard between the G, H, and B keys, and a microcontroller-based controller board that uses the Phillips TPM754 with the IBM firmware hard-coded into its ROM. The EasyPoint has three select buttons positioned below the keyboard–LEFT_MOUSE, RIGHT_MOUSE, and SCROLL–and a fourth button integrated into the EasyPoint itself. The EasyPoint defaults to two-button PS/2 mouse emulation for use with standard Windows PS/2 mouse drivers. It provides mouse “wheel” emulation, 3D pointer functions, and other advanced features when used with the IBM EasyPoint driver.

Hotkeys

Several hotkeys are supported using the computer keyboard. A hotkey is any key combination which uses the <Fn> key–one or more others to implement a function specific to the system. The MSIO recognizes hotkeys and either performs the desired function (if it is controlled by the MSIO) or generates an SMI to indicate to the system BIOS the particular hotkey that was pressed. The BIOS then performs the requested function.

External Keyboard/Mouse Communications

Pointing Device Initialization

When the PS/2 mouse is powered on, it sends 0xAAh, then 0x00h.

Data Format

The data transmitted by the pointing device to the system consists of the X, Y coordinates of the pointer and status of the buttons. This data is transmitted in a 3-byte serial PS/2 data packet that is compatible with the Microsoft PS/2 mouse.

Serial PS/2 data, illustrated in Figure 8-1, is transmitted to the system using the following parameters:

- Data bits8 bits
- Start bits 1 bit
- Stop bits 1 bit
- Parity 1 bit, odd

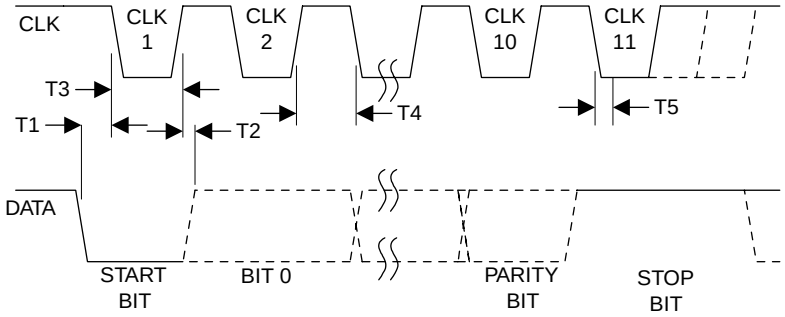

Figure 8-1. *PS/2 Data Transmission Sequence*

Communication between the computer system and the external keyboard or mouse is bidirectional. The keyboard controller of the computer system controls both KBDDATA and KBDCLK for status signaling. When the keyboard is idle or between scan code transmissions, both KBDCLK and KBDDATA are set high.

Keyboard/Mouse-to-System Transmissions

PS/2 keyboards and PS/2 mice use the same data protocol. The following discussion applies to both devices. Before the beginning of a transmission, the keyboard must check the status of KBDDATA and KBDCLK. A low KBDCLK indicates keyboard inhibition, and all keystrokes are loaded into the keyboard buffer. A low KBDDATA indicates the computer system is issuing a request-to-send (RTS) command. When the computer system issues an RTS, the keyboard loads all keystrokes into the buffer and prepares to receive data.

The keyboard begins transmission when both KBDDATA and KBDCLK are high. Data transmissions consist of a start bit, 8 data bits, an odd parity bit, and a stop bit. The keyboard first sets the correct level on KBDDATA and then pulses KBDCLK low. After the transmission, the system makes KBDCLK low until the transmitted data is

processed.

During a keyboard transmission, the computer system can request a transmission interrupt by lowering KBDCLK. The keyboard checks the state of KBDCLK every 100 microseconds during a transmission. If the line is detected low and the parity bit has been clocked out, the keyboard finishes the transmission. If KBDCLK is detected low before the rising edge of the parity bit is clocked out, the keyboard aborts the transmission. All data aborted during a transmission is sent later.

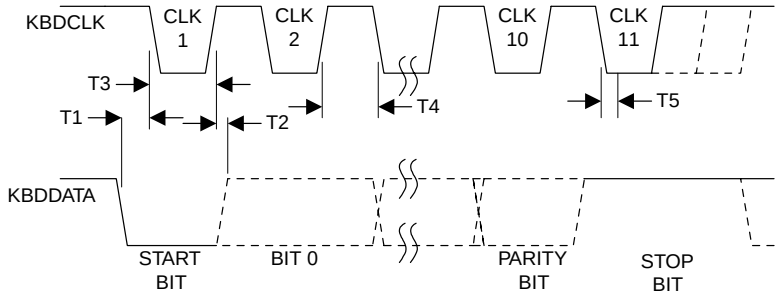

Figure 8-2. *Timing Diagram for Keyboard-to-System Transmissions*

System-to-Keyboard/Mouse Transmissions

The computer system has several commands that it may issue to the keyboard or mouse at any time. When the keyboard or mouse is transmitting to the computer system, the system first clamps the KBDCLK signal line to request a keyboard or mouse transmission halt. To ensure that the keyboard or mouse recognizes the interface request, the KBDCLK line must remain low (0) for at least 100 microseconds. If the keyboard or mouse transmission is past the rising edge of the parity bit clock pulse, the keyboard or mouse completes its transmission; if not, the keyboard or mouse loads the data into the character buffer and receives the data from the computer system.

Figure 8-3 shows the timing diagram for system-to-keyboard or -mouse transmissions.

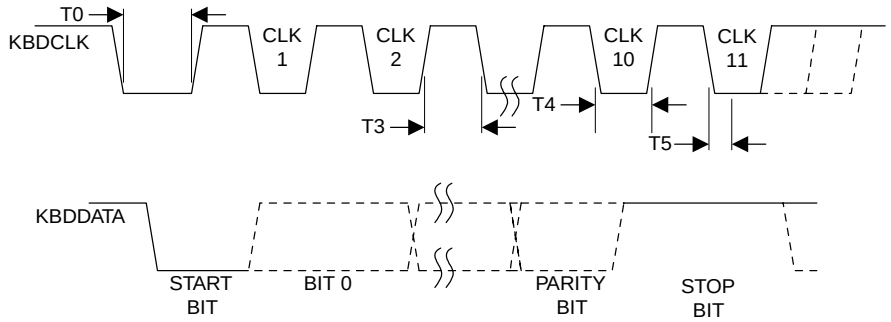

Figure 8-3. *Timing Diagram for System-to-Keyboard/Mouse Transmissions*

When the system is ready to transmit a command to the keyboard or mouse, it sets the DATA line low (0). This action serves as both an RTS and a start bit. Upon detecting the KBDDATA line low, the keyboard or mouse sets the KBDCLK line low, causing the start bit to be clocked out of the system. The interface then places the least-significant bit (LSB, data bit <0>) on the KBDDATA line, and the keyboard or mouse clocks out the LSB on the next negative going clock pulse. This process continues until all 8 data bits are clocked out of the interface.

After all data bits are clocked out of the interface, the system places an odd parity bit on the KBDDATA line. The keyboard or mouse repeats its clocking of the parity bit as before. The keyboard or mouse then sets the KBDDATA line low and clocks this line to the system for a stop bit. When the keyboard or mouse receives the stop bit, the interface sets the KBDCLK line low to inhibit the keyboard or mouse while it is processing the received data.

After the external device receives a controller command, the external device returns an ACK code (0xFAh) to the controller. If a parity error or timeout occurs, a resend command (0xFEh) is sent to the keyboard controller.

chapter 9

POWER SUPPLY

The Armada E500 and Armada V300 computers are designed to operate from multiple power sources, including an internal IBA-2 main battery pack. This requires a flexible power subsystem with advanced power management features. The main components of the power subsystem are:

- DC/DC converter: generates system voltages of +3.3 volts, +5 volts, and +12 volts, from a DC input (AC Adapter, Automobile Power Adapter/Charger, Aircraft Power Adapter, or Li-ion battery)
- Display inverter: generates voltages necessary for the LCD display backlight
- 8051 power management controller: microcontroller that manages all aspects of the power subsystem (integrated in the MSIO)
- I^2C Serial Bus Controller: communicates with the smart batteries subsystem (integrated in the MSIO)

Power sources for Armada E500 and Armada V300 are:

- Battery: The computers use product-specific 'smart' battery packs. The Armada E500 supports a 9-cell Lithium Ion (Li-ion) battery pack that plugs into the battery bay or DualBay, and a 6-cell Li-ion battery pack in the MultiBay; supporting up to three battery packs in the computer at one time. The V300 supports a 9- or 6-cell Li-ion primary battery pack in the battery bay, dependent on the computer model, and a 6-cell Li-ion battery pack in the MultiBay.
- AC Adapter: The AC Adapter provides a constant voltage output of 18.5 volts at 50 watts, and can fully charge the 9-cell battery within 3 hours with the system on. The AC Adapter is external to the computer enclosure.
- External DC source: Both computers can be powered by two other types of external DC sources. The Aircraft Power Adapter supplies power to the system, but does not allow charging of the batteries. The Automobile Power Adapter/Charger supplies power to the system and also allows charging of the batteries.

The computers have the following Power Management features:

- Standby modes
  - Local Standby: Selected subassemblies and subsections enter a reduced power mode after prescribed periods of inactivity.
  - Global Standby: All subassemblies enter a reduced power mode and some are powered off. This mode may be activated by system inactivity, a low battery condition, or manually by the operator. Resume from Standby is typically less than 5 seconds.
  - Hibernation: Activated when the system battery reaches a low battery condition. Hibernation must be enabled in Setup but can also be user initiated. Resume from Hibernation requires the longest latency.
- Power Conservation Utility Support
- Battery Fuel Gauge Utility

The primary battery is not warm-swappable; that is, it may not be exchanged unless there is another battery or AC power attached.

All main batteries are smart batteries; that is, they contain circuitry to communicate their charge state, total capacity, battery type, and other parameters to the system. This circuitry is typically accurate to about 1 to 2 percent after a complete charge or discharge cycle calibrates the gas gauge.

DC/DC Converter

The DC/DC power supply is controlled by the SUSC#_3 signal from the Southbridge (PIIX4M). The DC input from the AC Adapter, DC source or battery is converted into the following DC outputs: +2.5 volts @ 1.0 amp; +3.3 volts @ 5 amps; +5 volts @ 4 amps; and +12 volts @ 0.150 amp. Total output power is rated at 20 watts continuous and 35 watts peak. The input current of the power supply is limited by a 7 amp-rated fuse.

The main DC/DC controller is the Maxim MAX1630. It is a dual-synchronous buck converter. One of the buck converters generates the +5 volt output, while the other generates +3.3 volts and +12 volts. The +12 volts is generated off an auxiliary winding from the 3.3 volt-inductor.

The +VIDCORE output is generated off the + 3.3 volt output, using a linear regulator.

The DC/DC converter also provides a PGOOD_3 signal, which indicates all DC to DC outputs are operating properly with no over-voltage or under-voltage conditions. PGOOD_ includes VR_PWRGOOD_, which is the indication that the voltage regulator is within regulation.

The time delay for PGOOD_3 from the de-assertion of SUSC#_3 is about 100 milliseconds during the initial power on sequence. PGOOD_3 remains high in Power-On Suspend (POS), but is de-asserted in Suspend-to-RAM (STR). When resuming from STR, the time delay for PGOOD_3 from the de-assertion of SUSB#_3 is about 10 milliseconds.

Smart Battery

The smart batteries contain a microcontroller and EEPROM that track the battery history. From the battery history the pack can determine its capacity more accurately. Communication with the packs is via the I^2C bus using standard I^2C protocol, with the battery acting as a slave device. However, Compaq has implemented a scheme within the I^2C specification that allows the slave battery to signal the system that attention is required.

The smart pack is responsible for its own charge and discharge cycles. The battery must request permission to charge from the system. If permission is granted, the pack will control its own charging. When charging is complete, the pack will notify the system that it is done. Only one pack can be charged in the system at any time.

When using the constant voltage architecture while allowing battery charging at the same time, an over current limit is needed to keep within the AC Adapter's power limit. The system board has a 2.7 amp detection circuit, which will de-assert MBAT each time more than 2.7 amps is drawn. When MBAT is de-asserted, the new IBA2 battery packs will begin to throttle back on the amount of current/power it needs to charge the battery. This cycle can be repeated until an equilibrium is reached, thus keeping within the AC Adapter's power limit.

The Armada E500 and Armada V300 only support the IBA2 battery packs. The battery bay is mechanically keyed to allow only the newer IBA2 packs to be plugged in.

The IBA2 packs also incorporate a calibration feature that notifies the user that the packs should be calibrated. The Armada E500 and Armada V300 architecture supports calibrating of the packs by disallowing MBAT control from the external power source (de-asserting ADPTR_EN_5), and allowing the battery to power the system.

A low-battery detection point is programmable in the battery pack. The power management controller will set this level based on system configuration. If a battery discharges to this low-battery point, it will signal the system that attention is required.

Battery Priority

If two batteries are installed in a system, the power controller *always* charges and discharges in the same order. This priority scheme ensures that the user can always unplug all options and walk away with the highest charge possible in the main battery.

Charge Order:

1. Main battery
2. Dualbay battery
3. MultiBay battery
4. Expansion Base battery

Discharge Order:

1. MultiBay battery
2. Dualbay battery
3. Main battery

MBAT (Master Battery)

MBAT is a common signal between all of the batteries. This signal is driven active by the power source (either of the two batteries or the AC Adapter) that is powering the system. If the device powering the system is removed MBAT will go inactive. When this occurs any battery in the system will supply power to the system for 4 seconds which will allow the 8051 microcontroller time to assign another battery as master. MBAT will always be asserted in a system whenever there is a power source available to power the system (i.e. either a battery or the AC Adapter).

Fuel Gauge

The system supports a fuel gauge for the battery pack. The fuel gauge is displayed on the LCD or CRT by activating a hotkey **Fn + F8** combination. It is removed by pressing the hot key sequence again.

Each battery pack has a built-in fuel gauge on the pack to display the current status of the battery's charge. The indicator provides fixed charge indicators of 0, 25, 50, 75, and 100 percent; the actual battery status is rounded off to one of these values. To save power, the gauge is an on-demand type of indicator; that is, the indicators will only light when the user presses a small membrane switch on the pack. The location of the gauge permits the user to view it while the battery pack is in the battery charger.

Display Inverter

The display inverter is physically located in the LCD display assembly. The inverter provides power for the LCD backlight, and decodes a low frequency input from the system board that controls the brightness of the backlight.

The brightness PWM control is from the MSIO. The PWM signal can go from 0% (minimum brightness setting however is 15%) to 100% (maximum brightness).

The on/off (BLON#) control for the inverter are from the ATI video controller. The signal meets the timings and sequence required for LCD panels.

External AC Adapter

The external AC adapter supplies DC voltage to the DC/DC converter board for use by the system to operate and/or charge the installed battery pack. The AC input requirements are as follows:

- Output capacity 50 watts continuous
- Input voltage 90-264 VAC (auto-switching)
- Frequency 47-63 Hz
- Input Power < 60 watts at 85 percent efficiency

The AC adapter also contains protection circuitry to ensure that the application of an input voltage below the minimum specified above will not cause damage to the adapter circuitry or cause failure of the input fuse.

The adapter simply outputs 19 volts at 50 watts continuous, 60 watts peak (2.8 amps output max). The DC input is a simple two-wire (ground and power) connection, and may be connected to a wide number of sources. Primary support is given to the airline adapter and automotive adapter, but consideration is given that virtually any supply may be connected to the input.

The AC/DC or DC input may be turned off by control of the CPU, by turning off a FET under control of the MSIO. This feature is to perform battery calibration.

Power Management Controller

The system power management is performed by the 8051 microcontroller that is integrated in the MSIO Super I/O device. The controller monitors the batteries, power, standby, and keyboard Fn switches, controls battery charging, provides a battery fuel gauge to the system, and indirectly turns the DC/DC converter On and OFF. The controller interfaces to the system logic through 14 mailbox registers in the MSIO.

The intelligence in the constant voltage circuit pivots around the voltage and current sensing logic. The circuitry consists of two voltage level comparators, two current level load comparators, an AC adapter charge/discharge FET pair and logic for battery charge and arbitration. The purpose of the voltage and current sensing circuitry is to:

- Detect if external power is present (AC or DC input) and initiate battery discharge
- Monitor current into the System and disable battery charge when the AC/DC limit is exceeded

Charger presence (AC presence) is detected with a voltmeter detecting 17.5 volts or greater on the power rail input. The output of the AC-present logic goes to the MSIO "Charger Present" input and also may assert MBAT. The "Current Flow" ammeter makes sure that a battery stack voltage of 17.5 volts will NOT falsely assert "Charger Present."

A DC input jack may be present on the computer, intended to be supplied by either an airline adapter or automotive adapter. The DC-present voltmeter checks for an external voltage input of 12 VDC or greater. When an external source of voltage is applied between 12 and 17.5 volts, the system recognizes the external input but will not allow the battery to charge.

Hysterisis is built into the comparator, so that simple connection to a car's electrical supply will not cause the DC presence to be lost during a sag in the line (for instance, during cranking of the engine).

The "Current Flow" ammeter prevents the battery from backfeeding the AC/DC or DC input jack. It prevents the battery voltage from falsely indicating either "Charger present" or "DC-present." This current direction circuit has the advantage of low power and heat loss using an active circuit. The system is protected from a failure on the charger or DC input.

The ammeter consists of a comparator across a 50 milliohm resistor, R16. The output of this comparator is not read anywhere by the system, but acts to enable FET Q4. With Q4 turned off, the battery voltage VBAT cannot backfeed to the VADP rail.

The ammeter may not detect current flows less than 125 mA. In the event that the current flow ammeter does not detect current flowing from the VADP rail to the VBAT rail (for instance, during CPU Suspend mode or OFF mode with no battery charging) the FET is turned off but the body diode will still conduct. Negligible power is lost and the VBAT rail still cannot feedback to VADP.

The Isurge ammeter senses when the AC/DC limit of 2.6 amps is exceeded. This ammeter initiates charge current adjustment by the IBA battery. When the total current from the VADP rail is sensed to be over 50 watts, the Isurge ammeter will deassert MBAT. When MBAT is deasserted, the battery will immediately quit charging and the load from the battery will be isolated from the AC adapter.

The 8051 also monitors the temperature sensors in the system. The microcontroller sends the temperature information to the host system via SMI or SCI. The 8051 controls the fans in the system via a PWM signal. A zero percent duty cycle will keep the fan off and a 100 percent duty cycle will run the fan at its full speed. Minimum start up time for the fan is 10 milliseconds. The Armada E500 and Armada V300 incorporate a 35 mm fan.

The computers support the ACPI system power and sleep states from S0 to S5.

chapter 10

MASS STORAGE

The Armada E500 and Armada V300 computers are equipped with an easily removable 4-, 6-, or 12-GB (dependent on model), AT-compatible, 2.5-inch UDMA capable hard drive and a 1.44-MB, 3.5-inch, AT-compatible diskette drive. They support a 24X CD-ROM module and an LS-120 module in the MultiBays. The Armada E500 also supports a 4X DVD-ROM drive module,

The preinstalled hard drive contains software that supports PC Cards, IrDA, multimedia, and other system features.

Hard Drive Subsystem

The drives are selected for their high performance, small size, low power operation, and high shock resistance. The hard disk drive is packaged with an adapter to a 44-pin connector, which allows the hard drive to be removable. The hard drive can be accessed easily through a removable cover on the bottom of the system.

A second hard drive in a removable module is also supported. The hard drive must be mounted in a MultiBay module to the 68-pin bay connector.

Hard Disk Interface

The hard drive interfaces to the main PCB using the following industry-standard 44-pin connector that interfaces directly to the main PCB, detailed in Table 10-1.

Table 10-1
Hard Disk Connector Pin Outs Assignments

Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
1	HRESET#	IN	Controller Reset	23	HDIOW#	IN	I/O Write Command
					STOP	IN	UDMA during data bursts
2	GND	-	Ground	24	GND	-	Ground
3	hard drive7	IN/OUT	Data bit 7	25	HDIOR#	IN	I/O Read Command
					HSTROBE	IN	DMA ready (UDMA data In bursts)
					HSTROBE	IN	Data strobe (UDMA data Out bursts)
4	hard drive8	IN/OUT	Data bit 8	26	GND	-	Ground
5	hard drive6	IN/OUT	Data bit 6	27	HIORDY	OUT	I/O Channel Ready
					DDMARDY#	OUT	DMA ready (UDMA data Out bursts)
					DSTROBE	OUT	Data strobe (UDMA data In bursts)
6	hard drive9	IN/OUT	Data bit 9	28	CSEL	IN	Cable Select
7	hard drive5	IN/OUT	Data bit 5	29	DMACK	IN	DMA Acknowledge
8	hard drive10	IN/OUT	Data bit 10	30	GND	-	Ground
9	hard drive4	IN/OUT	Data bit 4	31	HIRQ	OUT	Interrupt
10	hard drive11	IN/OUT	Data bit 11	32	Reserved	-	-
11	hard drive3	IN/OUT	Data bit 3	33	DA1	IN	Address bit 1
12	hard drive12	IN/OUT	Data bit 12	34	PDIAG#	IN/OUT	Passed Diagnostics
13	hard drive2	IN/OUT	Data bit 2	35	DA0	IN	Address bit 0
14	hard drive13	IN/OUT	Data bit 13	36	DA2	IN	Address bit 2
15	hard drive1	IN/OUT	Data bit 1	37	HDCS0#	IN	Drive chip select 0
16	hard drive14	IN/OUT	Data bit 14	38	HDCS1#	IN	Drive chip select 1
17	hard drive0	IN/OUT	Data bit 0	39	DASP#	OUT	Device Active Slave
18	hard drive15	IN/OUT	Data bit 15	40	GND	-	Ground
19	GND	-	Ground	41	VCC	-	Hard drive VCC
20	NC	Keypin	No Connect	42	VCC	-	Hard drive VCC
21	DMARQ	OUT	DMA Request	43	GND	-	Ground
22	GND	-	Ground	44	RSV01	-	Reserved

Diskette Drive Subsystem

The diskette drive is a 3.5-inch form factor, 11 millimeter high, 1.44-megabyte (formatted), AT-compatible drive. Selected for its extreme small size and weight, low power operation, and high shock resistance, the drive is capable of reading and writing 720 K (formatted) diskettes to maintain backward compatibility. Refer to the manufacturer's specification for more details.

The diskette drive is packaged in a module form for insertion into the Dualbay on the front of the Armada E500. The Armada V300 has a fixed diskette drive in the same location.

The diskette controller is software compatible with the Intel 82077 controller and is integrated into the MSIO Super I/O device. The controller is clocked by a 14.318-MHz clock and supports transfer rates of 125, 250, 300, 500, and 1000 kilobits/second.

The power-down mode is controlled by the issuance of the automatic power-down mode command to the diskette controller. The command's argument specifies what the minimum power-on time is before the device attempts to enter the power down mode (the system BIOS programs this timeout to be 0.5 second). The criteria for automatically entering power down mode are:

- All motor enables are inactive
- INT output is low
- The device is idle (as signified by the IDLE output being high)

If, after the BIOS issues the auto-power-down command, the above criteria are met, then 500 milliseconds later the diskette controller enters power-down mode. If the criteria are not satisfied when the power-down timer expires, the diskette controller postpones the process until the criteria are met.

When power-down mode is successfully entered, the PD output goes active high, and the FDC tri-states its diskette drive interface. The IDLE pin continues to be high after power-down mode is entered. The internal crystal oscillator cannot be disabled in power-down mode due to the long time necessary for stabilization of the oscillator output on a restart.

CD-ROM Module

The minimum speed of the CD-ROM drive module is 24X. The CD-ROM mates to the 68-pin MultiBay connector on the both computer series.

DVD-ROM Module

The minimum speed of the DVD-ROM drive module is 4X. The DVD-ROM mates to the 68-pin MultiBay connector on the Armada E500 computer.

SuperDisk LS-120 Drive Subsystem

The LS-120 drive option is a bootable device. The drive uses an imbedded ATAPI (IDE) controller for the host interface. The drive is capable of reading and writing to standard SuperDisk LS-120 diskettes, industry-standard 1.44 MB and 720 KB 3.5-inch diskettes and 1.7 MB Distribution Media Formatted diskettes (read only), and 1.2 MB diskettes.

Table 10-2
LS-120 Diskette Formats

	120 MB	1.7 MB DMF	1.44 MB	1.2 MB	1.2 MB	720 K
Minimum Total Formatted Capacity (Bytes)	125,958,144	1,720,320	1,474,560	1,261,568	1,228,800	737,280
Sector Size (Bytes)	512	512	512	1024	512	512
Minimum Total Number of Sectors	246,527	3360	2880	1,232	2400	1440
Magnetic Tracks/Surface	1736	80	80	77	80	
Optical Servo Tracks/Surface	900	N/A	N/A	N/A	N/A	N/A
Sectors per Track	51-92	21	18	8	15	9
Sector Interleave	1:1	2:1	1:1	1:1	1:1	1:1
Number of Reassignable Spare Sectors	170	0	0	0	0	0
Number of Zones (Each Side)	55	1	1	1	1	1

chapter 11

INTERNAL MODEM AND INTERNAL COMBINATION MODEM/NIC

This chapter describes the internal Compaq high-speed modems used in the Armada E500 and Armada V300 computers. These computers support the internal combination Compaq 56K (V.90) plus Intel PRO/100+ Mini-PCI Modem or the Compaq Global Mini-PCI 56K (V.90) Modem, both with Lucent Technology chipsets. The modem is CTO configurable and a user upgrade.

Combination Card Overview (Lucent Chipset)

The combination Compaq 56K (V.90) Plus Intel PRO/100+ Mini-PCI Modem consists of a 10/100Mbps NIC section and a V.90 modem section. These two functions, shown in Figure 11-1, are combined to present only one PCI load to the host system. In addition to sharing the host interface, the NIC and modem share a single EEPROM.

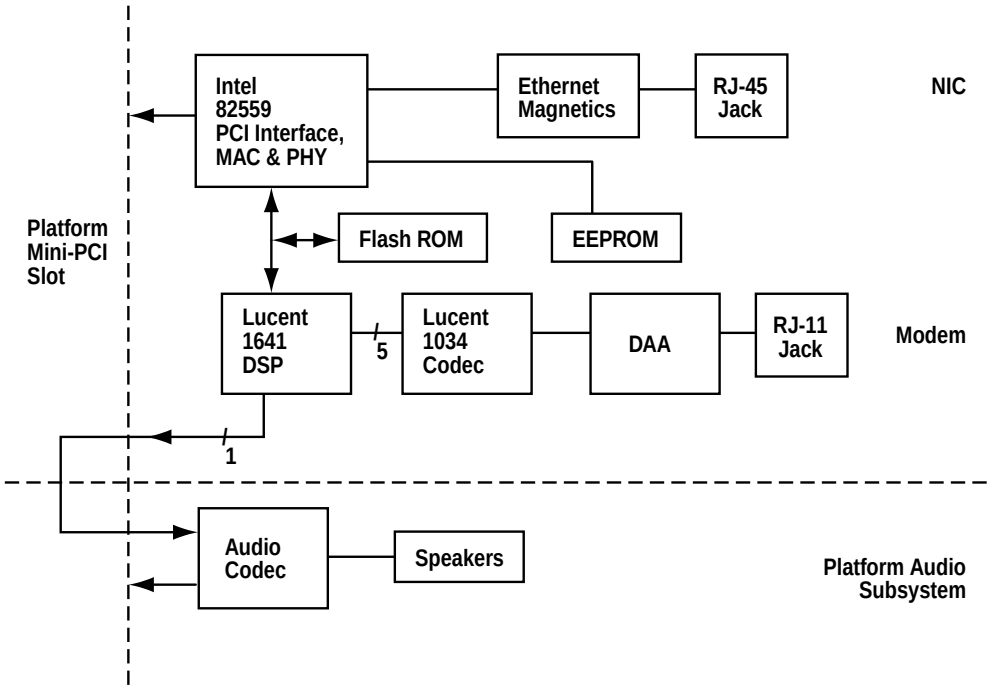

Figure 11-1. *Armada E500 and Armada V300 Combination Modem/NIC Block Diagram*

Network Interface

The heart of the network interface portion of the card is the Intel 82559. It provides all LAN functions between the mini-PCI Bus and the Ethernet interface magnetics. The PCI configuration register information is stored in a serial EEPROM for host initialization. A 64-kB Flash ROM sharing the modem port of the 82559 allows execution of PXE code and Boot-on-LAN functionality.

Network Interface Components

Intel 82559

The 82559 is a highly integrated device based on previous Intel 8255x chips. Features include:

- Glueless 32-bit PCI bus master interface
- Integrated 10/100 LAN MAC
- Integrated 10/100 LAN PHY
- Multiplexed I/O port for modem DSP and Flash ROM support
- CLKRUN# support
- Wake on LAN (WOL) support
- SMB interface for total cost of ownership (TCO) and wired for management (WfM) support

Network Interface Magnetics

- Provide 1500 Vrms minimum isolation

RJ45 Jack

- Shielded for EMI
- Short leads for compliance with Mini-PCI specifications
- Two LEDs located on jack
  - Yellow LED: ON indicating LINK; Flicker ON representing activity; OFF indicating no activity
  - Green LED: ON indicating 100 Mbps link; OFF representing 10 Mbps link

Ethernet Driver Requirements

Ethernet Features

- 10 Mbps Ethernet: IEEE 802.3 standard 10 Base T
- 100 Mbps Ethernet: IEEE 802.3u standard 100 Base TX
- Full duplex at 10 and 100 Mbps
- Auto-Negotiation
- Wake on LAN from all power-managed sates, including soft off (S5)
- Low Power State on Link Loss

Data Link Layers

- IEEE 802.2 LLC
- SNAP

Software Support

- Artisoft Lantastic 7.0, 8.0, Dedicated Server 1.1
- Banyan 7.x, 8.5x
- DEC Pathworks 4.x, 5.x
- IBM LAN Server version 1.2, 1.3, 2.0, 4.0
- Microsoft NT 3.51, NT 4.0, Windows 2000
- Novell Netware 3.1x, 4.x, 5.x

Protocol Support

- TCP/IP
- Novell IPX/SPX and Microsoft compatible
- Novell IPX ODI
- Microsoft NetBEUI
- Sun Microsystems PC-NFS
- Banyan Vines Ethernet
- Pathworks v4.1, 5.0 Ethernet
- IBM DLC

Modem

This modem portion of the card is a controller-less design utilizing the Lucent Technologies chipset. A ROM-coded 3.3-volt DSP1641 digital signal processor performs signal processing and provides an interface to the CODEC. The 3.3-volt CSP1034C is a high precision sigma-delta CODEC. It provides support for digital tuning of the hybrid circuit. The DAA is a transformer-based design with worldwide country support.

Modem Components

Lucent 1641 DSP

The main components for the 1641 DSP are:

- 3.3-volt Lucent 1600 DSP core
- Internal ROM and RAM
- VALV34 register interface
- JTAG interface
- PLL
- Two serial I/O channels
- 16550 MIMIC
- ISA host interface

Lucent CSP1034 CODEC

The CSP1034 CODEC performs the analog-to-digital and digital-to-analog conversions for the modem line signals and has a digital interface for connection to the 1641 DSP. CODEC features include:

- High precision sigma delta A/D, D/A converters
- Support for “real” or “complex” impedance countries

Modem Data Access Arrangement

- Hook relay circuit
  - The DAA contains one relay circuit to handle on/off hook.
- DC holding coil
  - The DAA interface consits of an active DC holding circuit, often called a “dry” transformer configuration.
- Ring detection circuit
  - The ring signal detection frequency range and cadence is variable, depending upon the country the modem is selected for
- Loop disconnect (pulse) dialing
  - The DAA contains an additional relay for pulse dialing, which shunts the holding circuit
- Current limiting
  - The DAA has additional current limiting circuitry to meet the requirements for CTR21

Modem Call Progress Audio

This modem utilizes the platform audio subsystem and speakers to provide audible call progress during a data connection. The call progress signal is scaled digitally in the modem data pump according to the speaker level setting (ATL 1, L2, L3) and then is transferred to the audio subsystem as a pulse width-modulated signal.

Modem Digital Line Guard

To meet the requirement for over-current protection on the telephone line, the modem has incorporated circuitry to sense whenever the current on the line exceeds approximately 130 milliamps, and should immediately go back on hook and emit an audible warning tone. This sensing should occur whenever the modem is off hook, not just at the beginning of a phone call.

Wake-up on Ring

The modem can wake up a host system from a low power state, but not S4 or S5, with the presence of an incoming ring signal. This is accomplished by generating a PME# assertion on the PCI bus. The PME# assertion for the modem will be generated by the 82559, as it is for LAN wake-up events.

Modem Driver Requirements

Data Mode Capabilities

- V.90 (a-law, mu-law)
- K56flex (a-law, mu-law)
- V.8bis
- V.80
- V.42bis, MNP5
- V.42 (LAPM, MNP2-4)
- V.34 (file date: 10/96)
  - Optional symbol rates: 2800, 3429
  - Asymmetric symbol rates
  - Synchronous primary channel data signaling rates: 33600, 31200
  - Automatic rate renegotiation
  - 32, 64 state trellis encoding
- V.32bis
- V.32
- V.23
- V.22bis
- V.22
- V.21
- Bell 212A
- Bell 103J

Fax Mode Capabilities

- TIA-578-A (Class 1)
- T.30
- T.4 (Group 3)
- V.17
- V.29
- V.27ter
- V.21 Channel 2

Command Set

- V.250 (Partial)
  - TIA-602
  - Identification: +GMI, +GMM, +GMR
  - Port control: +IPR, +ICF, +IFC, +Ilrr
  - Modulation: +MS, +MR, +MA
  - Error control: +ES, +ER, +EB, +ESR, +ETBM
  - Data compression: +DS, +DR

Power Management

The combination modem/NIC card derives its power from either the main PCI +3.3-volt supply or the +3.3 volt AUX supply. A “smart” switch on the card senses the supply source and switches between the two supplies as the host system transitions between a low-power state (S4, S5) and a higher power state (S0 - S3). The +3.3-volt AUX will only be present in the system when the notebook is on AC

Because the +3.3-volt AUX supply can appear and disappear in changing system power states, it is necessary that both the modem and NIC sections of the card be capable of returning their associated hardware pieces into low-power states.

Power management of the card must account for the separate, but interrelated, pieces of the modem and NIC functions. For example, if the modem is programmed to wake up the system on ring in the D3 state but the LAN is not being used, a portion of the 82559 must be awake to generate a PME. At the same time, as much as possible of the Ethernet sections of the device should be powered down. The NIC and modem together do not draw more than 200 milliamps from the +3.3-volt AUX supply in the S4 and S5 states, per the Mini-PCI specification.

Operating System BIOS Support

Compaq Power Management Extensions for Windows NT

- Windows NT 4.0

APM - Revision 1.2

- Windows 95
- Windows 98

ACPI

- Windows 98
- Windows 2000

Modem/NIC Power States

Table 11-1
NIC Power States

State	Activity	Power Consumption @ 3.3 V
D0	Full functionality	< 600mW
D1		
D2		
D3 hot	LAN PME enabled	< 600mW
D3 hot	LAN PME disabled	< 600mW

The following table maps the ACPI-defined power states (general, system, and device) to the expected platform wake-up capabilities:

Table 11-2
NIC Wakeup Power States

ACPI State		Description	Wakeup Capability
G0	[D0]	Full On (Working)	Not Applicable
G1 (S1/S2)	[D1/D2]	Lite Sleep (Standby)	Resume to previous working state
G1 (S3)	[D3 hot]	Sleep (Suspend)	Resume to previous working state
G1 (S4)	[D3 cold]	Deep Sleep (Hibernation)	Resume to previous working state
G2 (S5)	[D3 cold]	Soft Off	Boot/IPL (fresh start)
G3		Mechanical Off	Not Applicable

Note: There are three different results expected for wakeup scenarios: no response, software resume, and system boot/IPL.

Table 11-3
Modem Power States

State	Activity	Power Consumption @ 3.3 V
D0	DSP, crystal, PCI bus active	< 260mW
D3 hot	Crystal disabled; DSP stopped; PCI bus active	< 55mW
D3 cold	Crystal disabled; DSP and PCI bus stopped; PME# capable of being asserted	< 6mW

Note: The D1 state is not defined for a modem device. Although D2 is defined, VCOMM (in Windows) does not support D2; thus the modem transitions to a pseudo D2 state using the value in the S89 register. The default transition time is 10 seconds.

Variances will occur between different computers and between different operating systems. The information below does not apply to all computers that the modem is install.

Table 11-4
Modem Sleep State Transitions

G0 (S0) (Working) → G1 (Sleeping), Or → G2 (S5) Soft Off	Modem Activity	Comments
User Initiatives through Alt-F4 or Suspend	Inactive (D2), COM port may be open or closed	The system will go to S1 or S3 depending upon the system implementation and capabilities reported by the ACPI BIOS. For example, it might go directly to S1 or S3 or it might try to go to S3 first but if a device/driver doesn't support it, then it will go to S1. The modem will go to D3 hot (if S1) or D3 cold (if S3).
	Awake (D0)	See above.
	Online/transferring data	The system will ignore the request.
OS timer	Inactive (D2); COM port may be open or closed	The system will go to S1 or S3 depending upon the system implementation and capabilities reported by the ACPI BIOS. For example, it might go directly to S1 or S3 or it might try to go to S3 first but if a device/driver doesn't support it, then it will go to S1. The modem will go to D3 hot (if S1) or D3 cold (if S3).
	Awake (D0)	See above.
	Online/transferring data	The system will ignore the request
Low battery	Inactive (D2)	In Windows 98 the system will go to S1 or S3 depending upon the system implementation and capabilities reported by the ACPI BIOS. In Windows 2000 the system is capable of going to S1, S3, S4 or S5. The modem will go to D3 hot (if S1) or D3 cold (if S3, S4, or S5).
	Awake (D0)	(see above)
	Online/transferring data	(see above)
Thermal shutdown	Inactive (D2)	The system will transition to S1, S3, S4, or S5 depending upon which state the buttons are assigned to. The modem will go to D3 hot (if S1) or D3 cold (if S3, S4, S5).
	Awake (D0)	See above.
	Online/transferring data	See above.
User depresses Power or Sleep buttons	Inactive (D2); COM port may be open or closed	The system will transition to S1, S3, S4, or S5 depending upon which state the buttons are assigned to. The modem will go to D3 hot (if S1) or D3 cold (if S3, S4, S5).
	Awake (D0)	(see above)
	Online/transferring data	The system will ignore the request.

When the system is in the working state, G0 (S0), and a communications program is running, the modem will either be in D0 or D2 and is capable of detecting an incoming call. See Table 11-5 for the other states. Note that the modem's COM port must be open at the time the computer is put into one of the sleep states in order to detect an incoming call.

Table 11-5
Modem Wake Up State Transitions

G1 (Sleeping) → G0 (S0) (Working)	System Sleep State			
Modem State	**S1**	**S3**	**S4**	**S5**
D3 hot	Modem detects an incoming call and wakes up the system.			
D3 cold		Modem detects an incoming call and wakes up the system.	Modem will not detect an incoming call.	Modem will not detect an incoming call.

Remote LAN Management

Remote LAN management is performed using several different industry standard methods. The legacy three-pin header implementation is not supported by mini-PCI. Note that many of these features are only available in ACPI-compliant systems.

Wake on LAN

The wake-on-LAN (WOL) function is implemented using standard wake up events to trigger PME# assertion, as outlined in the *PCI Bus Power Management Interface Specification 1.1*. These wake up events as defined in the *Network Device Class Power Management Specification* are:

- Change of network link state
- Receipt of a network wake-up frame (packet filtering)
- Receipt of a Magic Packet

WOL is supported only in S3, whether it is in the stand-alone or docked configuration.

The OS must enable PME# on the 82559 before the card is placed into the D3 state.

Boot on LAN

Boot-on-LAN support relies on PXE code resident in the flash ROM and the boot methods specified above to allow remote administration of the host system. Boot on LAN is determined during BIOS POST.

Global Mini-PCI Modem Card (Lucent Chipset)

Modem Overview

This modem, shown in Figure 11-2, is a controller-less design utilizing the Lucent Technologies Mars2 chipset. A ROM-coded DSP1646 digital signal processor performs the signal processing and interfaces to the system bus. The CSP1034C is a high-precision sigma-delta CODEC. It provides support for digital tuning of the hybrid circuit. Call progress audio is routed to the audio subsystem by way of a pulse-width modulated signal from the DSP 1646.

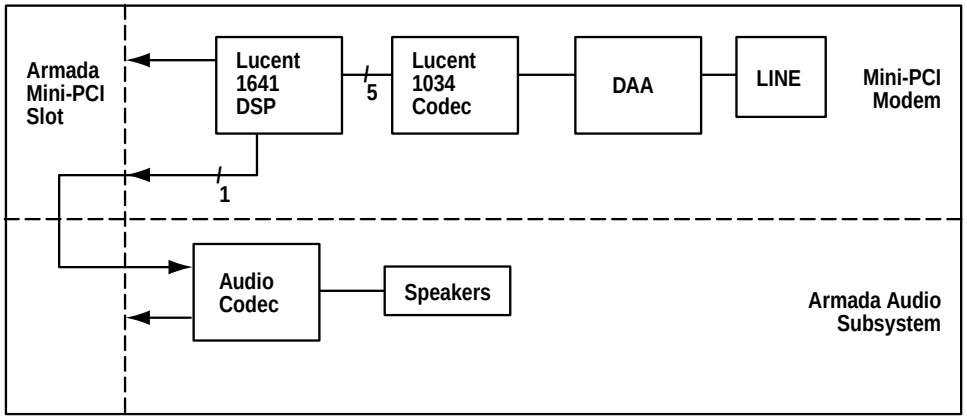

Figure 11-2. *Mini-PCI Card Block Diagram*

Modem Chipset

This modem is based on the Lucent 1646 DSP and the 1034C CODEC. The main components of the 1646 DSP are:

- ROM-coded digital signal processor
- Two full-duplex bus master streams
- Internal PLL
- 24-bit I/O channels
- 16550 UART (MIMIC)
- PCI decode logic

Modem Data Access Arrangement

The data access arrangement (DAA) contains one relay circuit to handle on- or off-hook. The DAA interface consists of an active DC holding circuit, often called a “dry” transformer configuration. Ring signal detection frequency range and cadence is variable, depending upon the country the modem is selected for. The DAA contains an additional relay for pulse dialing, which shunts the holding circuit. Additional DAA circuitry limits the current, to meet the requirements for CTR21.

Modem Call Progress Audio

This modem utilizes the platform audio subsystem and speakers to provide audible call progress during a data connection. The call progress signal is scaled digitally in the modem data pump according to the speaker level setting (ATL1, L2, L3) and then transferred to the audio subsystem as a pulse-width modulated signal.

Modem Digital Line Guard

To meet the requirement for over-current protection on the telephone line, the modem has incorporated circuitry to sense whenever the current on the line exceeds approximately 130 milliamps, and should immediately go back on hook and emit an audible warning tone. This sensing should occur whenever the modem is off-hook, not just at the beginning of a phone call.

Modem Driver Requirements

Data Mode Capabilities

- V.90 (a-law, mu-law)
- K56flex (a-law, mu-law)
- V.8bis
- V.80
- V.42.bis, MNP5

- V.42 (LAPM, MNP2-4)
- V.34 (file date: 10/96)
  - Optional symbol rates: 2800, 3429
  - Asymmetric symbol rates
  - Synchronous primary channel data signaling rates: 33600, 31200
  - Automatic rate re-negotiation
  - 32, 64 state trellis encoding
- V.32bis
- V.32
- V.23
- V.22bis
- V.22
- V.21
- Bell 212A
- Bell 103J

Fax Mode Capabilities

- TIA-578-A (Class 1)
- T.30
- T.4 (Group 3)
- V.17
- V.29
- V.27ter
- V.21 Channel 2

Command Set

- V.250 (Partial)
  - TIA-602
  - Identification: +GMI, +GMM, +GMR
  - Port control: +IPR, +ICF, +IFC, +Iirr
  - Modulation: +MS, +MR, +MA
  - Error control: +ES, +ER, +EB, +ESR
  - Data compression: +DS, +DR
- V.251

Modem Power States

For information on the Mini-PCI modem power states, modem sleep state transitions, and/or modem wakeup state transitions, refer to Tables 11-3 through 11-5.

appendix *A*

DOCKING

The Compaq Armada E500 computer is compatible with the ArmadaStation EM docking station, Convenience Base, and Port Replicator. The Armada V300 computer docks with the Port Replicator only.

Docking Sequence

Docking is first detected when the EBOXL# pins (long pins) make contact with the docking station. The EBOXL# signal is de-asserted, and an interrupt is generated by the 8051. The 8051 then polls EBOXS# (short pins) to ensure that a complete connection has been made.

Next, the I^2C bus to the docking interface is enabled, and the EEPROM ID in the docking station is read to determine which type of docking station is connected. Depending on the type of docking station connected, different control signals will be enabled to pass the correct set of signals out to the attached docking station. For a complete description of the docking sequence, please refer to the BIOS specification.

Docking Interface

From a control signal perspective, there are several types of signals that pass through the 176-pin connector. The three main types of signals are:

- Direct pass through: power, parallel port, some audio signals, video, most FDD signals
- Switched signals: PCI bus, expansion PCI clock, USB port 0, PS2, I^2C
- MUXed signals:
  - ArmadaStation EM mode: Reset, some FDD signals, serial port, AC link

The quick switches are controlled by the 8051 microcontroller for all docking instances, except when docked to the ArmadaStation EM, the circuitry within the docking station controls the PCI bus and expansion PCI clock quick switches.

The Armada Station EM is designed to utilize the Intel MPCI2 PCI to PCI bridge to perform the connecting and disconnection of primary PCI bus. The MPCI2 incorporates a docking state machine that is capable of monitoring system status, controlling electrical isolation, issuing docking event interrupts, and performing motor mechanism controls. A set of control and status pins is provided specifically for detecting docking connection and controlling quick switches for the dock and undock operations. In the ArmadaStation EM design, the firmware is only used to initiate the execution of the MPCI2 and then the entire operation is carried out solely by the MPCI2 through its state machine to complete the connect or disconnect of the primary PCI bus.

MPCI2 uses two status pins, CD1# and CD2#, to monitor the status of docking connection. The CD1# and CD2# status pins, when asserted, indicate to MPCI2 that the docking connector of the notebook and docking station are fully coupled. MPCI2 begins executing its docking state machine once these pins are sampled low. The CD1# and CD2# pins are connected to a GPO pin of the Tempest micro-controller. This allows the ArmadaStation EM firmware to initiate the docking sequence under command of notebook's micro-controller.

appendix B

POWER CONSERVATION

The Armada E500 and Armada V300 power conservation features are designed to extend operating time while running in either the normal operating "On" mode or the reduced power "Suspend" (also referred to as "Global Standby" or "System Standby") mode under either AC power or internal battery power.

Power Management States

The system has four distinct hardware power management states and a number of additional firmware states. A hardware state is defined to be a unique system configuration, during which some combinations of components are powered on while the rest are powered off or in a disabled state. The two most obvious hardware states are On, in which all components are powered, and Off, in which the minimal number of components are powered.

The four states are defined as follows:

- **On**–All components in the system receive power. This is the state that the system is in when it is in full operation. There are a number of firmware sub-states that define component usage. For example, the CPU clock may be throttled while in the On state, thereby giving the user the illusion that the system is running when, in fact, it is in a power savings mode.
- **Standby**–Almost all components in the system receive power. The exceptions are the hard disk and the bay device (either diskette drive or CD-ROM). The clock generator is on and the LCD backlight inverter is turned off. The clock to the CPU is stopped, placing the CPU in the Stop Clock state. Exit from Standby is immediate, and any external or internal activity brings system to full On state. Possible activity includes PS/2 ports, keyboard press, CardBus/PCMCIA, or any button activity.

- **Suspend**–Only those devices required for data retention and integrity receive power. These devices include system DRAM, Video DRAM, 3D RAGE LT Pro Video Controller, all 82443BX power planes, a small part of the PIIX4M, and the MSIO. This mode offers the lowest power consumption available while maintaining the present state in DRAM. If Suspend to Disk has been selected in the Setup Menu, the present state of the machine is saved to disk, and the machine is put in the Off state. Pressing the Suspend/Resume button is not considered a cold power on if Suspend to Disk has been selected but a Resume, where the last state of the machine is loaded from the disk.
- **Off**–the minimal number of components receive power. These devices include the RTC and the MSIO Super I/O controller. The previous state of the machine is lost when the system enters the Off state, but all setup information, RTC, EEPROM data, and CMOS data is retained. Exit from the Off state to the On state is accomplished by pressing the Suspend/Resume button and is considered a cold boot.

  Hibernate–Included in the Off state is 0 volt Suspend (Suspend-to-Disk). The BIOS writes to a protected area of the hard drive all register and memory contents necessary for data retention and then turns the system Off as described above. On a power On, the system checks to see if the last event was a 0 volt Suspend. If so, it restores the contents of all the registers and memory, and the system resumes. This allows an infinite Suspend life. Both the Suspend and Resume operations are lengthy due to the hard drive accesses.

Transitions between these states are based on external switches, internal and external events, and timeouts. All switches on the computer are inputs to the MSIO. The MSIO debounces the switch inputs and presents them to the 440BX chipset. The different mechanisms for transitions from one state to another are enumerated below:

- **Suspend/Resume switch–**This switch is an input to the MSIO and can be used as either Suspend/Resume or to turn the system completely Off. A switch press by itself indicates a Suspend/Resume. Holding the <Fn> key while pressing the switch indicates a request to the OS to turn the system Off (requires OS support). When used without the <Fn> key, depressing the switch transitions the system between On and Suspend. Holding the switch in for four or more seconds causes the system to go to Off directly without OS intervention. Once the system is in the Off state, a switch press restarts the system.
- **Lid switch**–The lid switch input to the MSIO provides an SMI input to the PIIX4M. The lid switch can provide a Suspend/Resume function.
- **Ring Indicate on serial port–**The RS-232 chip is on the Suspend power plane to enable the pass through of a modem ring to the MSIO. A transition on the RING# pin wakes up the MSIO, which toggles the PIIX4M causing the system to return to On if the system is currently in Standby and this feature has been enabled in Setup.

- **Ring Indicate–**The system must be in Standby for this feature to operate. The modem card passes through the modem ring to the RING# pin. The MSIO then wakes up the PIIX4M.
- **RTC Alarm–**An alarm causes the IRQ8# from the RTC to assert and wake the PIIX4M. The PIIX4M generates an SMI to cause the system to return to On if the system is currently in Suspend or Standby. The E500 and V300 are fully ACPI compliant and supports the Wake-on-Day-of-Month feature.
- **Low battery voltage**–The 8051 microcontroller in the MSIO monitors the main battery voltage with an A/D channel using a moving average algorithm. At a predetermined voltage level, the MSIO generates low voltage SMIs that warn the user that the battery is getting low. A second voltage level is set so that if the user has not suspended the system by that point, the MSIO generates an external SMI to force the system to suspend. A third voltage level is set so that if the battery level continues to drop to the point where the system cannot remain in Suspend-to-RAM mode, the system performs a Suspend-to-Disk and then shuts down completely.

Processor Power Management

The processor is a significant source of power dissipation. Because of this, there are several ways in which power drain to the CPU can be reduced. There are four power states supported by the processor, as shown in Table B-1.

Table B-1
Processor Power States

State	Description	Power Level
On	Full power state	100%
Auto Halt	HALT instruction executed	12.1%
Quick Start	STPCLK# asserted, acknowledged	5%
Deep Sleep	Stop CPU clock after entering Stop Grant state	1%

The Full-On state is the normal state for the processor. It is executing at 100% of the rated clock frequency. The power in this state varies depending on the instruction mix.

The Auto Halt state is entered via software by executing the Halt instruction. Once executed, the processor is in a low-power state and cannot execute any additional instructions. Return to the On state is accomplished by generating an interrupt to the processor. Asserting STPCLK# can NOT change the state of the processor. In order to get to the Quick Start or Deep Sleep state, an interrupt must first bring the processor to the Full-On state. APM (advanced power management) uses the Halt instruction to save power during times when there is no heavy system activity.

The Quick Start state is entered by asserting the STPCLK# signal to the processor. The processor completes the current transaction, generates a Stop Grant special cycle, and then stops its internal clocks. Return to the Full-On state is done by de-asserting the STPCLK# signal. The STPCLK# signal is driven by the chipset.

This signal is driven dynamically when used for "clock throttling." Throttling, which is used to lower system power, simulates running the processor at a slower speed by periodically entering the Quick Start state. This state is also used during Standby, but only as a way to get to the Deep Sleep state.

The Deep Sleep state can only be entered from the Quick Start state. Once the CPU has generated a Quick Start special cycle and moved the Quick Start state, stopping the CPU clock input causes the CPU to enter the Deep Sleep state. To return to Full-On, the CPU clock must be restarted and remain stable for 1 millisecond. This returns the processor to the Quick Start state. From there, the return to full on is completed by de-asserting the STPCLK# signal. Deep Sleep state is used only during Standby because of the 1 millisecond latency.

Processor Thermal Management

The processor temperature is monitored by the CPUTEMP signal. This signal is an analog signal whose voltage level indicates temperature and is monitored by the MSIO. There are three temperature levels that are set in the EEPROM.

- Crossing the first temperature level causes the CPU to enter thermal management. The cooling fan is turned on ("passive-before-active" cooling). If the temperature drops 5 degrees below this level, the CPU returns to full speed.
- If the temperature continues to rise and exceeds the second (higher) temperature level, the system sets the CPU to 50 percent speed using clock throttling.
- If the temperature exceeds the third temperature level, the system is forced into a Critical Suspend.

Secondary Cache Power Management

The MP2 module handles secondary cache power management functions. The L2 cache is powered down during Off and S3 Suspend modes.

PCI Bus Power Management

The Armada E500 and Armada V300 computers use the method defined in the PCI 2.1 specification to reduce the power used by the PCI bus. This method uses a PCI signal called CLKRUN# to stop the PCI clock when no PCI activity is occurring.

Video Power Management

The RAGE Mobility-P graphics controller has several internal timers that monitor subsystems within the video controller. When one of these areas becomes inactive for a long period of time, the controller disables that area, saving overall system power.

RAGE Mobility-P power management logic supports four device power states: On, Standby, Suspend, and Off. Each power state can be achieved by software control bits, hardware pins, or hardware timers. By implementing power management capability registers in PCI configuration space, the chip becomes directly controllable from the system BIOS. Three dedicated pins (CLKRUN#, AGP_BUSY#, and STP_AGP#) give full controllability of the PCI and AGP bus interface to the system chipset.

Clocks to every major functional block (2D, 3D, video, LCD out, TV out, primary display pipe, secondary display pipe) are controlled by a dynamic clock switching technique that is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is significantly reduced during normal operation. If the clock is needed, it can be restored within one clock without affecting overall performance of the chip.

Hard Drive and Bay Power Management

Both the internal hard drive and the bay power are controlled by the PIIX4M. These signals are de-asserted during the Standby state to remove power from the internal hard drive and whatever module is in the bay.

A timer monitors hard drive activity. It can be set by way of the Setup program to spin down the hard drive and put it into a low-power state after a selected period of inactivity. The timer can be disabled or set to one of the predefined timeout periods.

MSIO Super I/O Power Management

The MSIO Super I/O Controller supports a low-power state that can be enabled by software. It also has internal power management for some of its functions. This internal power management is enabled at all times. The MSIO is placed into a low-power state during the Standby and Static Suspend modes.

Audio Power Management

The Maestro 2E has a low-power mode that can be entered from software. This mode is used in the Standby and Suspend states and when the notebook audio is disabled by way of the Setup program. There is an AUDIO_PWRDOWN signal that can be used to put the audio amplifier into a low-power state. The AUDIO_PWRDOWN signal is generated from the PIIX4M GPO3. This signal is used whenever the controller is placed into a low-power state as mentioned above.

Index

G

H

I

K

L

M

N

T

U

V

W

Z